

Reducing Dielectric Loss in $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ Ceramics by Spark Plasma Sintering-Enabled Control of Grain-Boundary Potential Barriers

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Abstract

$\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ (CCTO) ceramics exhibit a giant dielectric constant but often suffer from high dielectric loss that limits their practical use. In this work, Spark Plasma Sintering (SPS) was employed as a rapid, interface-aware densification route to regulate the microstructure and electrical response of CCTO without chemical doping. Dense ceramics were fabricated at 1000 °C under 50 MPa with holding times of 5–30 min and compared with a conventionally sintered reference prepared at 1100 °C for 12 h. The SPS samples showed finer and more homogeneous grains, reduced secondary-phase signatures, much lower dielectric loss, and a markedly stronger grain-boundary resistive response. The SPS-10 sample delivered $\epsilon' \approx 2.9 \times 10^4$ and $\tan \delta = 0.022$ at 1 kHz at room temperature. Impedance and nonlinear J-E analyses indicate that the superior dielectric behavior is consistent with more effective grain-boundary barriers in the SPS ceramics. Fracture-surface XPS is interpreted here only as supportive near-surface chemical information, rather than as direct proof of grain-boundary-specific defect chemistry. These results show that SPS can substantially suppress dielectric loss in CCTO by coordinating densification, microstructural refinement, and interfacial electrical response.

Keywords: Internal barrier layer capacitor, grain-boundary engineering, Schottky barrier, impedance spectroscopy, nonlinear current-voltage behavior

I. Introduction

The relentless miniaturization of electronic devices continues to drive demand for ceramic dielectrics that combine very high permittivity with acceptable loss and thermal stability. Among the candidate materials, calcium copper titanate, $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ (CCTO), has attracted sustained attention because it can exhibit a colossal dielectric constant over a broad temperature and frequency window^{1–4}. This unusual response is generally interpreted in terms of an extrinsic internal barrier layer capacitor (IBLC) mechanism rather than a conventional ferroelectric transition. In this picture, semiconducting grains are separated by comparatively insulating grain boundaries, and the contrast between these two regions governs the effective dielectric response^{3–5}.

Despite its attractive ϵ' , the practical use of CCTO is constrained by its relatively high dielectric loss, especially near room temperature and under low-frequency operating conditions^{6–7}. Reducing $\tan \delta$ without sacrificing the giant dielectric constant remains the central challenge in CCTO processing. Previous strategies have included compositional doping, post-annealing under controlled atmospheres, and tuning of the Cu-rich intergranular phase that accompanies sintering^{8–12}. These

approaches can be effective, but they also complicate compositional control and may introduce competing defect or secondary-phase effects.

An alternative route is to manipulate the microstructure and interfacial electrical response through the sintering schedule itself. SPS is attractive in this context because it couples rapid heating, short dwell time, and applied pressure, thereby enabling dense ceramics to be obtained with a much lower thermal budget than conventional sintering^{13–15}. For CCTO, such processing could simultaneously limit abnormal grain growth, restrain excessive Cu redistribution, and modify the effective barrier configuration that governs leakage and nonlinear transport. The objective of the present study is therefore to determine how SPS holding time influences phase evolution, microstructure, dielectric loss, impedance response, and nonlinear electrical behavior in CCTO ceramics. Importantly, the revised discussion treats fracture-surface XPS as supportive near-surface information and combines it with the structural and electrical data in a deliberately conservative manner.

Conventional solid-state sintering, the most common fabrication route for CCTO ceramics, typically requires high temperatures (≥ 1050 °C) and long holding times (several hours) to achieve adequate densification⁹. Such prolonged high-temperature exposure inevitably leads to extensive grain growth, sometimes resulting in abnor-

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mally large grains measuring hundreds of micrometers¹⁶. This coarse microstructure can be detrimental, and the high thermal budget can also lead to the volatilization of copper oxide, creating secondary phases and defects that contribute to increased dielectric loss¹⁷. In contrast, advanced sintering techniques offer new avenues for microstructural engineering. Spark Plasma Sintering (SPS) has emerged as a powerful and efficient method for consolidating a wide range of materials, including advanced ceramics^{18–19}. SPS utilizes a combination of uniaxial pressure and a pulsed DC current passed directly through the sample and graphite die, enabling extremely rapid heating rates and significantly shorter sintering times at lower temperatures compared to conventional methods^{13,20}. This rapid, non-equilibrium processing can effectively suppress grain growth, leading to fine-grained, highly dense microstructures¹⁴. Furthermore, the unique processing environment of SPS, including the plasma and electromagnetic fields, can influence the defect chemistry at interfaces, offering a unique handle to tailor the grain boundary properties.

This research paper investigates the use of Spark Plasma Sintering as a strategic tool to manipulate the grain boundary potential barriers in CCTO ceramics, with the ultimate goal of reducing dielectric loss. We hypothesize that by systematically varying the SPS holding time, we can achieve precise control over the grain size and, more importantly, the grain boundary state, including its defect concentration and structural integrity. This microstructural control, in turn, allows for the direct modulation of the grain-boundary potential barrier height. A comprehensive suite of material characterization techniques is employed to establish a clear and robust correlation between the SPS processing parameters, the resulting microstructure, the nature of the grain boundaries, the height of the potential barriers, and the final dielectric and electrical properties. By comparing SPS-fabricated samples with a conventionally sintered counterpart, this work aims to demonstrate that SPS is not merely a rapid densification technique but a sophisticated method for engineering grain boundary interfaces to produce high-performance CCTO ceramics with a desirable combination of giant permittivity and low dielectric loss.

II. Materials and Methods

(1) Powder synthesis

High-purity $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ (CCTO) powder was synthesized with the conventional solid-state reaction

method. The starting materials were calcium carbonate (CaCO_3 , 99.9 % purity, Sigma-Aldrich), copper (II) oxide (CuO , 99.9 % purity, Alfa Aesar), and titanium (IV) oxide (TiO_2 , anatase, 99.8 % purity, Sigma-Aldrich). These powders were weighed in stoichiometric proportions corresponding to the $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ formula. The mixture was subsequently subjected to high-energy ball milling (Fritsch Pulverisette 7) in a zirconia vial with zirconia balls for 12 hours using ethanol as the milling medium to ensure homogeneous mixing. After milling, the resulting slurry was dried at 80 °C for 24 hours in a drying oven. The dried powder was ground gently in an agate mortar and then calcined in an alumina crucible at 950 °C for 12 hours in an ambient air atmosphere with a heating and cooling rate of 5 K/min. The calcination step was repeated once with intermediate grinding to ensure complete reaction and phase formation, a standard procedure for achieving phase-pure CCTO powder¹¹. The phase purity of the synthesized powder was confirmed by X-ray diffraction prior to the sintering process.

(2) Sintering procedures

The calcined CCTO powder was divided into five batches for different sintering experiments. Four batches were sintered using a Spark Plasma Sintering system (SPS, FCT Systeme GmbH, HP D 25), while one batch was prepared using conventional sintering (CS) to serve as a baseline for comparison. For SPS processing, approximately 3 grams of the CCTO powder was loaded into a 20-mm diameter graphite die and punches, with graphite foil used to separate the powder from the die walls and punches. The sintering was carried out under a vacuum of approximately 10 Pa. A uniaxial pressure of 50 MPa was applied at the beginning of the cycle and maintained throughout the sintering and cooling process. The temperature was ramped up to a target of 1000 °C at a rate of 100 K/min. The sintering temperature was chosen to be below the typical temperatures used in conventional sintering to leverage the advantages of SPS in promoting densification at lower thermal budgets²¹. To investigate the effect of processing time on the microstructure and properties, the holding time at 1000 °C was varied. The four SPS samples prepared are hereafter designated as SPS-5, SPS-10, SPS-15, and SPS-30, corresponding to holding times of 5, 10, 15, and 30 minutes, respectively. After the holding period, the pulsed DC current was turned off, and the samples were allowed to cool down naturally within the SPS chamber. The sintering parameters are summarized in Table 1. For the conventional sintering process,

Table 1: SPS and CS parameters for $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ ceramic samples.

Sample ID	Sintering Method	Temperature (°C)	Holding Time (min)	Pressure (MPa)	Atmosphere
SPS-5	Spark Plasma	1000	5	50	Vacuum
SPS-10	Spark Plasma	1000	10	50	Vacuum
SPS-15	Spark Plasma	1000	15	50	Vacuum
SPS-30	Spark Plasma	1000	30	50	Vacuum
CS-1100	Conventional	1100	600	-	Air

the CCTO powder was uniaxially pressed into a 20-mm-diameter pellet at 200 MPa, followed by cold isostatic pressing at 300 MPa. The green pellet was then sintered in a muffle furnace at 1 100 °C for 10 hours in an ambient air atmosphere, with heating and cooling rates of 5 K/min. This sample is designated as CS-1100.

(3) Electrical property measurements

For electrical measurements, the polished ceramic pellets were coated with silver paste on both parallel surfaces to form electrodes, followed by firing at 600 °C for 30 minutes to ensure good ohmic contact. The dielectric properties (ϵ' and $\tan \delta$) were measured as a function of frequency (10^2 Hz to 10^6 Hz) and temperature (from -100 °C to 200 °C) using a Novocontrol Alpha-A high-performance frequency analyzer²².

Complex impedance spectroscopy (IS) measurements were carried out using the same instrument over the frequency range of 10^{-1} Hz to 10^6 Hz at room temperature (25 °C) with an applied AC voltage of 100 Mv²³. The resulting data were presented as Nyquist plots (Z'' vs. Z') and analyzed using ZView software with an equivalent circuit used to separate grain-associated and grain-boundary-associated responses^{24–25}. When the fitted resistive and capacitive terms were reported in geometry-normalized form, the conversions $\rho = RA/L$ and $C_s = CL/A$ were used, where A is the electrode area and L is the sample thickness.

The non-linear current-voltage (I-V) characteristics were measured at room temperature using a Keithley 2450 SourceMeter. The DC voltage was swept from 0 to 100 V across the samples²⁶. From the I-V data, the non-linear coefficient (α) and breakdown electric field (Eb) were determined. The breakdown field was defined as the field at which the current density reached 1 mA/cm². The grain boundary potential barrier height (Φ_B) was calculated from the I-V data based on the thermionic emission model for Schottky barriers²⁷.

III. Results and Discussion

(1) Phase composition and crystal structure

The phase purity and crystal structure of the synthesized CCTO ceramics were investigated using X-ray diffraction. Fig. 1 shows the XRD patterns for the conventionally sintered CS-1100 sample and the SPS-sintered samples with different holding times (SPS-5, SPS-10, SPS-15, and SPS-30). All major diffraction peaks can be indexed to the body-centered cubic perovskite-related structure of CCTO, confirming successful phase formation. The SPS samples, particularly SPS-5 and SPS-10, show sharp peaks with no detectable secondary phases within the XRD detection limit. In contrast, the CS-1100 sample exhibits weak reflections attributable to CuO and TiO₂. Rather than assigning these phases to a single mechanism, we consider them to be the combined result of the prolonged high-temperature treatment: Cu volatilization and local non-stoichiometry can destabilize the nominal CCTO composition, while Cu-rich intergranular segregation during sintering and cooling can further promote detectable secondary-phase residues^{11–12,28–29}. The

very weak CuO feature emerging for SPS-30 suggests that even at 1 000 °C, extended holding begins to offset the phase-purity advantage of the shorter SPS cycle.

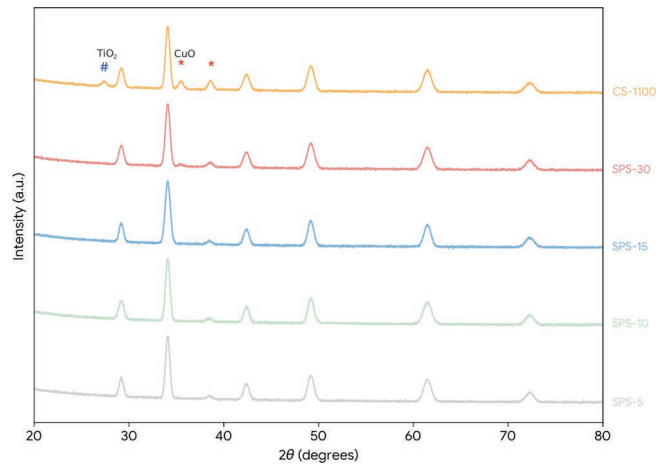


Fig. 1: XRD patterns of CCTO ceramics prepared by conventional sintering (CS-1100) and Spark Plasma Sintering with different holding times (SPS-5, SPS-10, SPS-15, SPS-30).

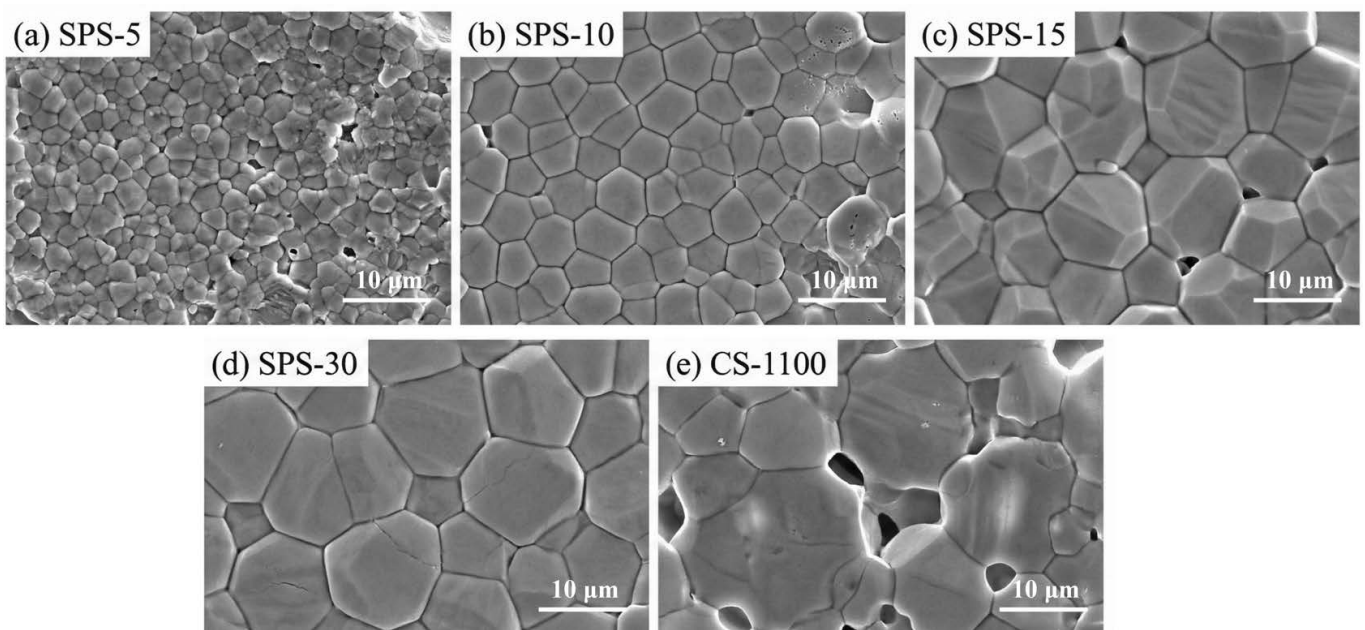
Rietveld refinement was performed on the XRD data to extract quantitative structural information, and the results are summarized in Table 2. The refinement results show excellent agreement between the observed and calculated patterns, with low goodness-of-fit (χ^2) values, confirming the structural model's accuracy. The lattice parameter *a* is found to be very similar across all samples, ranging from 7.391 Å to 7.393 Å, which is consistent with reported values for CCTO³⁰. The refinement confirms the presence of minor secondary phases (CuO and TiO₂) in the CS-1100 sample, constituting approximately 1.8 % and 0.5 % by weight, respectively. The SPS-30 sample shows about 0.6 % CuO, while the other SPS samples were determined to be phase-pure within the detection limit of the XRD technique. This structural analysis provides the first piece of evidence that SPS processing offers superior control over phase purity compared to conventional sintering, which is a critical factor influencing dielectric loss.

(2) Microstructure and density

The microstructures of the fracture surfaces of the CCTO ceramics were examined by FESEM, and the results are presented in Fig. 2. A dramatic difference in microstructure is immediately apparent between the conventionally sintered and SPS-sintered samples. The CS-1100 sample exhibits a very coarse-grained microstructure, characterized by abnormally large, irregularly shaped grains with sizes often exceeding 50 μm. This is a common feature of conventionally sintered CCTO, where extended high-temperature exposure promotes significant grain growth, often mediated by a liquid phase¹⁵. The microstructure also shows evidence of some porosity trapped at the grain boundaries. In stark contrast, all SPS samples display a much finer and more uniform grain structure. The SPS-5 sample has a very fine-grained microstructure with an average grain size of approximately 1.5 μm. As the holding time increases from

Table 2: Rietveld refinement results for CCTO ceramics sintered under different conditions.

Parameter	SPS-5	SPS-10	SPS-15	SPS-30	CS-1100
Space Group	Im-3	Im-3	Im-3	Im-3	Im-3
Lattice Parameter, a (Å)	7.3915(2)	7.3918(3)	7.3921(2)	7.3925(4)	7.3931(3)
Unit Cell Volume (Å ³)	403.98	404.03	404.08	404.15	404.25
CCTO Wt. (%)	>99.9	>99.9	>99.9	99.4	97.7
CuO Wt. (%)	<0.1	<0.1	<0.1	0.6	1.8
TiO ₂ Wt. (%)	<0.1	<0.1	<0.1	<0.1	0.5
Rwp (%)	6.54	6.81	6.65	7.02	7.15
χ^2	1.25	1.31	1.28	1.40	1.45

**Fig. 2:** FESEM micrographs of the fracture surfaces of CCTO ceramics: (a) SPS-5, (b) SPS-10, (c) SPS-15, (d) SPS-30, and (e) CS-1100.

5 to 30 minutes, a clear and systematic grain growth is observed. The average grain size increases from 1.5 μm for SPS-5 to 3.2 μm for SPS-10, 5.8 μm for SPS-15, and 9.7 μm for SPS-30. This demonstrates that SPS holding time is an effective parameter for controlling grain size in a predictable manner¹⁴. The grains in all SPS samples are densely packed with well-defined grain boundaries and significantly less porosity compared to the CS-1100 sample.

The quantitative results of the density and average grain size measurements are summarized in **Table 3**. All SPS-sintered samples achieved high relative densities, exceeding 97 % of the theoretical density, even with a short holding time of 5 minutes. The density slightly increases with holding time, reaching a maximum of 98.8 % for the SPS-30 sample. This high level of densification at a relatively low temperature (1 000 °C) and in a very short time is a hallmark of the SPS technique, attributed to enhanced diffusion kinetics under the combined effects of pressure and pulsed current²⁸. The CS-1100 sample, despite being sintered at a higher temperature and for a much longer time, only reached a relative density of

95.2 %, likely due to the entrapment of pores during the rapid growth of large grains.

Table 3: Physical properties of sintered CCTO ceramic samples.

Sample ID	Bulk Density (g/cm ³)	Relative Density (%)	Average Grain Size (μm)
SPS-5	4.93	97.0	1.5 $\pm$ 0.4
SPS-10	4.98	97.9	3.2 $\pm$ 0.8
SPS-15	5.01	98.5	5.8 $\pm$ 1.5
SPS-30	5.03	98.8	9.7 $\pm$ 2.1
CS-1100	4.84	95.2	65.3 $\pm$ 25.1

The grain size distribution for each sample was analyzed and is presented as histograms in **Fig. 3**. The distributions for the SPS samples are relatively narrow and unimodal, becoming broader as the holding time increases

and the average grain size grows. The SPS-5 and SPS-10 samples show particularly tight distributions, indicative of a highly homogeneous microstructure. In contrast, the grain size distribution for the CS-1100 sample is extremely broad and multimodal, reflecting the inhomogeneous nature of the abnormal grain growth process²⁹. This pronounced microstructural difference, particularly the ability of SPS to produce dense, fine-grained, and homogeneous ceramics, is expected to have a profound impact on the electrical and dielectric properties.

(3) Grain boundary structure and chemistry

To gain deeper insight into the interfacial structure relevant to the IBLC mechanism, TEM analysis was conducted on the SPS-10 and CS-1100 samples, representing two microstructural extremes. Fig. 4 shows that the SPS-10 sample contains clean and sharp interfaces between adjacent grains, and the corresponding SAED pattern confirms the crystallinity of the CCTO matrix. By contrast, the CS-1100 sample displays thicker and less well-defined interfacial regions, with local disordered layers in the order of 2–3 nm. These observations are consistent with a microstructure in which prolonged conventional sintering promotes stronger intergranular

phase redistribution, likely involving a Cu-rich transient liquid and subsequent disordered boundary remnants after cooling^{11–12,27}. Such interfacial inhomogeneity can broaden the distribution of local barrier properties and create additional leakage pathways, whereas the sharper SPS interfaces are more compatible with a narrower and more effective barrier distribution.

The chemical state of titanium and oxygen on the fracture surfaces was examined by means of XPS. In the present study, these spectra are interpreted as near-surface chemical information obtained from fractured surfaces, not as direct, grain-boundary-specific measurements. Fig. 5 shows the high-resolution Ti 2p and O 1s spectra. The Ti 2p envelopes of all samples can be deconvoluted into a dominant Ti^{4+} component and a lower-binding-energy contribution commonly assigned to Ti^{3+} . The relative Ti^{3+} signal is lower for the shorter-dwell SPS samples than for the conventionally sintered specimen. However, because the measurement averages over the exposed fracture surface and because the fracture mode was not independently quantified as purely intergranular, these differences should be regarded as comparative surface-sensitive trends rather than direct proof of the specific defect chemistry at the grain-boundary core.

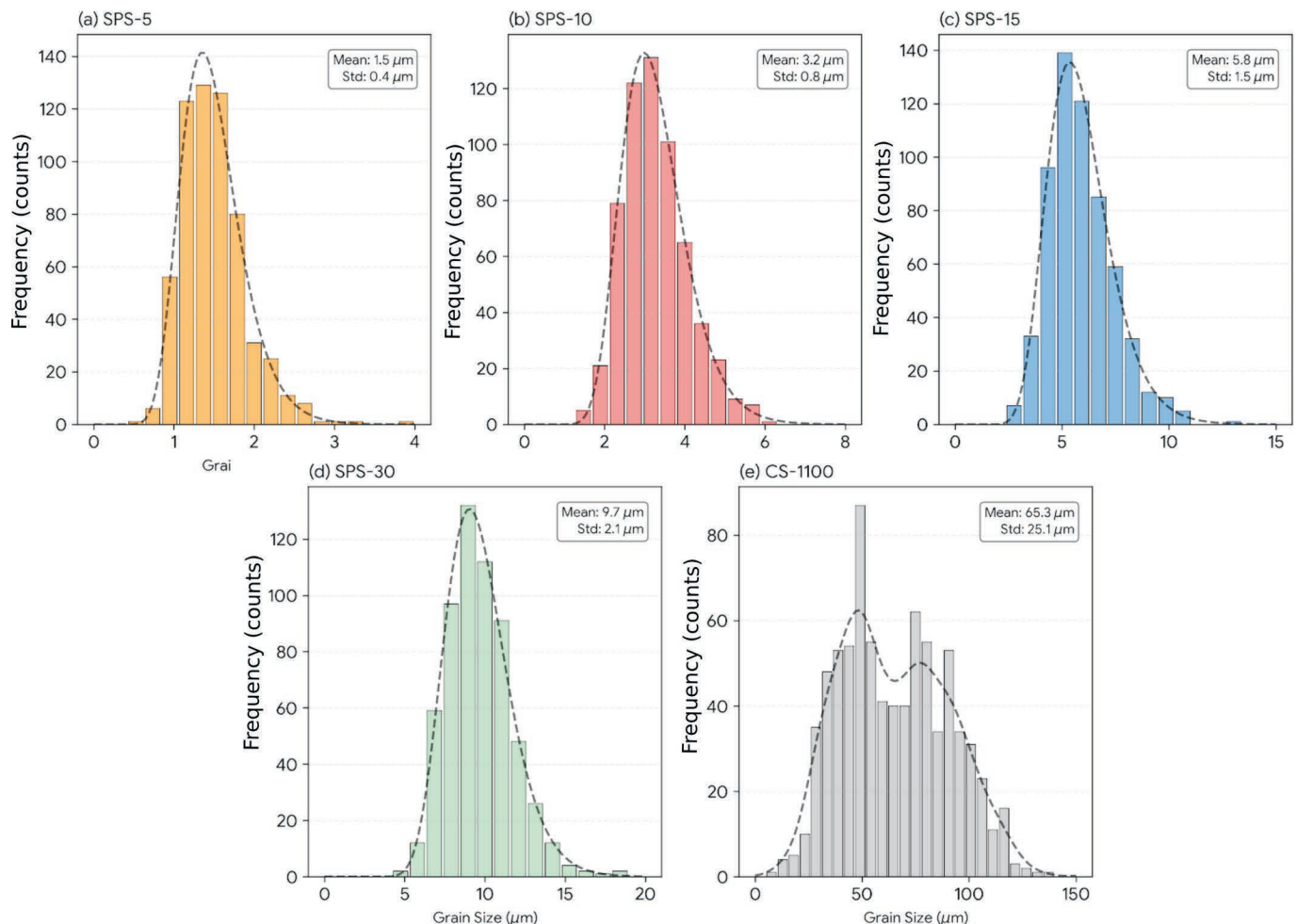


Fig. 3: Grain size distribution histograms for CCTO ceramics prepared under different sintering conditions: (a) SPS-5, (b) SPS-10, (c) SPS-15, (d) SPS-30, and (e) CS-1100. Author note for final artwork replacement: In panel (a), the x-axis label should read 'Grain Size (μm)'. The editable source figure was not available in the present workspace, so this note is included to guide the final figure replacement.

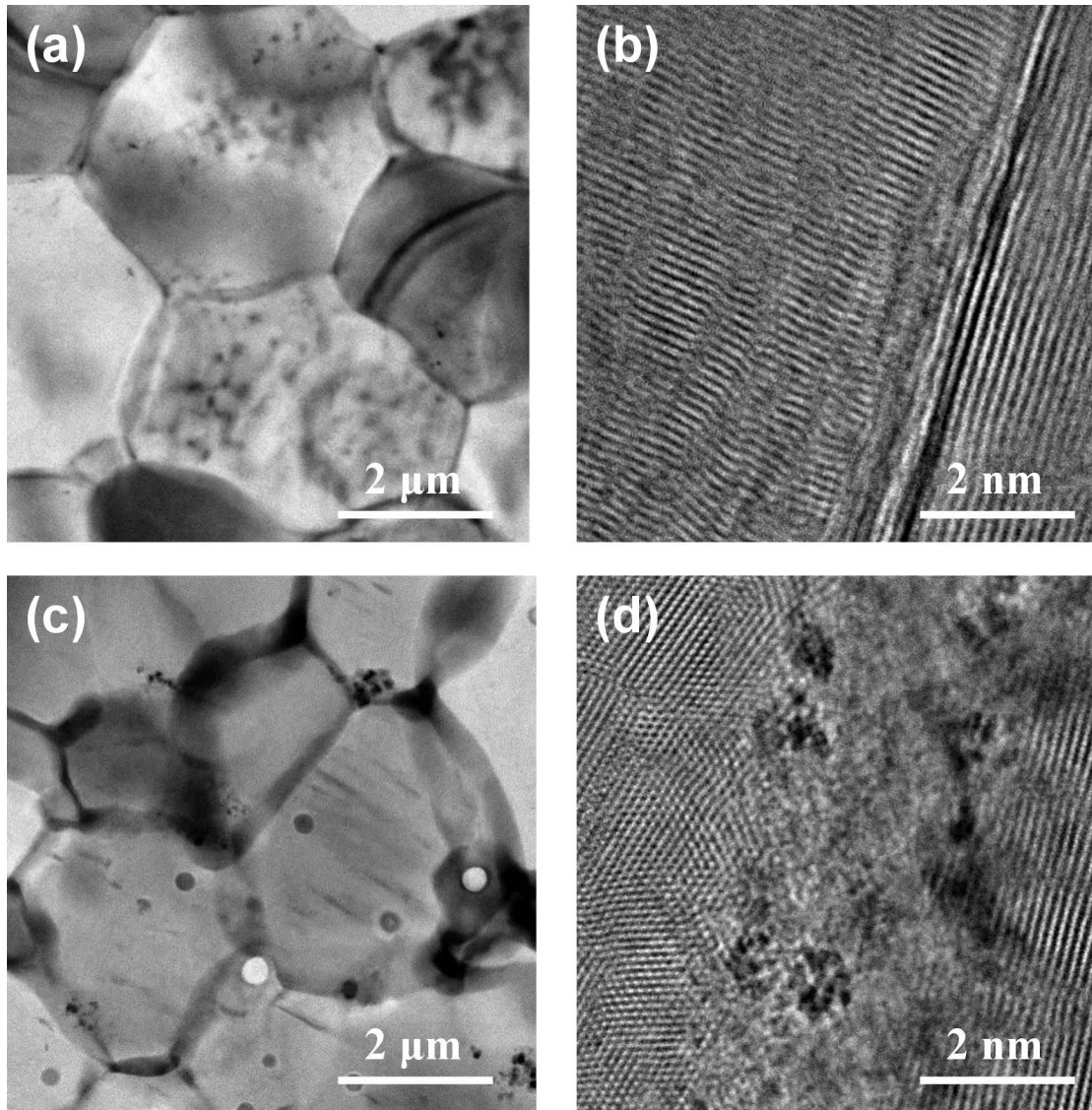


Fig. 4: (a) Bright-field TEM image of the SPS-10 sample. (b) HRTEM image of a representative grain boundary in the SPS-10 sample. (c) Bright-field TEM image of the CS-1100 sample showing a thicker grain boundary. (d) HRTEM image of a grain boundary in the CS-1100 sample revealing a disordered interfacial layer.

The O 1s spectra require similar caution. In oxide systems, the higher-binding-energy O 1s component near 531–532 eV is often more appropriately interpreted as oxygen residing in defect-rich, oxygen-deficient, hydroxylated, or otherwise non-equivalent local environments, rather than as a direct photoelectron signal originating from an oxygen vacancy itself^{31–32}. Accordingly, in the present work the ~531.2 eV feature is assigned to oxygen associated with oxygen-deficient or defect-rich near-surface environments on the fracture surface. Using conventional Kroger-Vink notation, oxygen vacancies are referred to here as V_O . The relative variation of this component, together with the Ti^{3+} signal, is qualitatively consistent with differences in defect-related electronic structure among the samples. Nevertheless, these spectra do not by themselves establish a quantitative grain-boundary vacancy concentration. We therefore use XPS only as supportive evidence that complements the XRD, TEM, dielectric, impedance, and nonlinear electrical results.

(4) Dielectric properties

The frequency dependence of the ϵ' and $\tan \delta$ for all CCTO samples was measured at room temperature, and the results are shown in Fig. 6. All samples exhibit the characteristic giant ϵ' of CCTO. At 1 kHz, the ϵ' value for the CS-1100 sample is approximately 48 000. The SPS-sintered samples also show high ϵ' values, which increase with holding time and grain size: from ~18 000 for SPS-5 to ~42 000 for SPS-30 at 1 kHz. This trend is consistent with the IBL model, where a larger grain size (and thus fewer grain boundaries per unit volume for a given thickness) often leads to a higher effective ϵ' ^{23,33}. All samples display a relatively stable dielectric plateau at lower frequencies, followed by a Debye-like relaxation drop at higher frequencies.

The most significant and technologically relevant result is observed in the dielectric $\tan \delta$. The conventionally sintered CS-1100 sample exhibits a high $\tan \delta$ of 0.18 at 1 kHz, which is typical of loss-prone CCTO ceramics³⁴. In contrast, all SPS-sintered samples show a pronounced

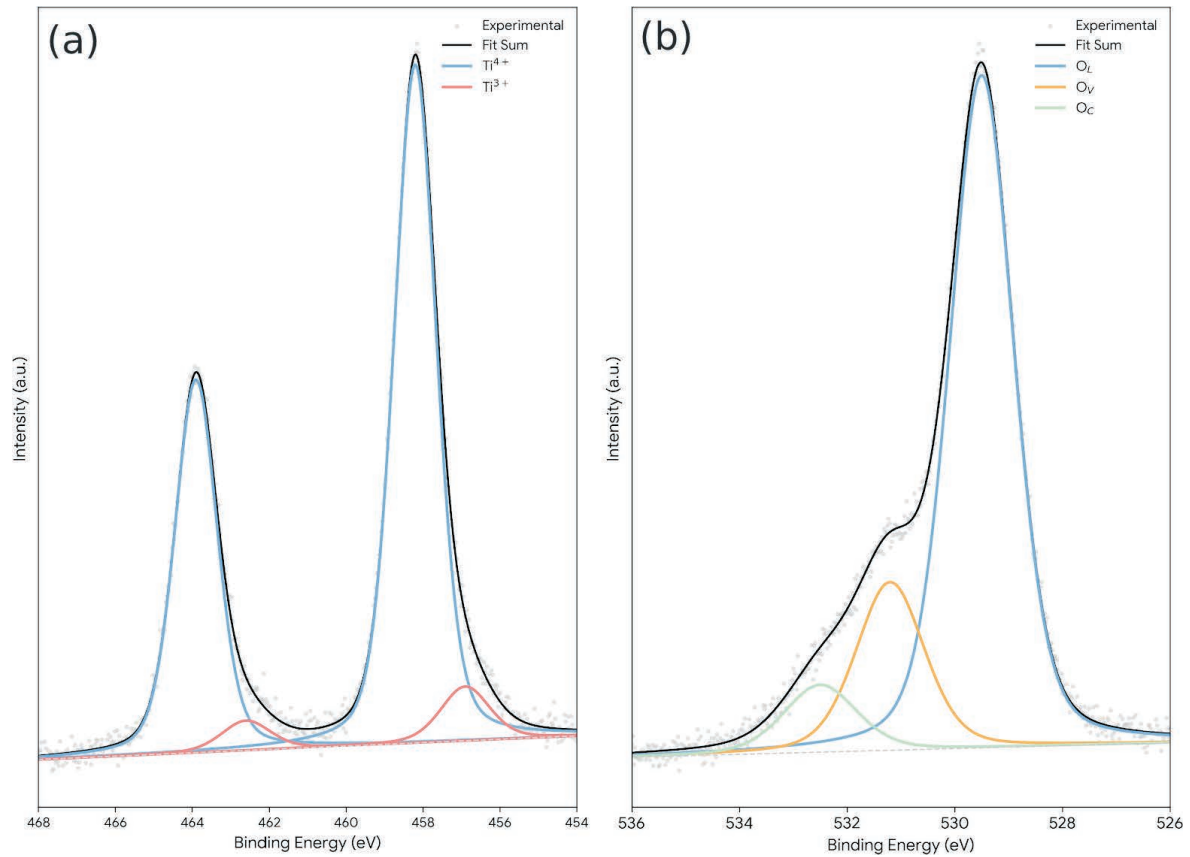


Fig. 5: High-resolution XPS spectra of CCTO ceramics. (a) Deconvoluted Ti 2p core-level spectra showing contributions from Ti^{4+} and Ti^{3+} states. (b) Deconvoluted O 1s core-level spectra showing contributions from lattice oxygen (OL), a higher-binding-energy component assigned to oxygen in defect-rich or oxygen-deficient near-surface environments, and chemisorbed oxygen or carbonate species (OC).

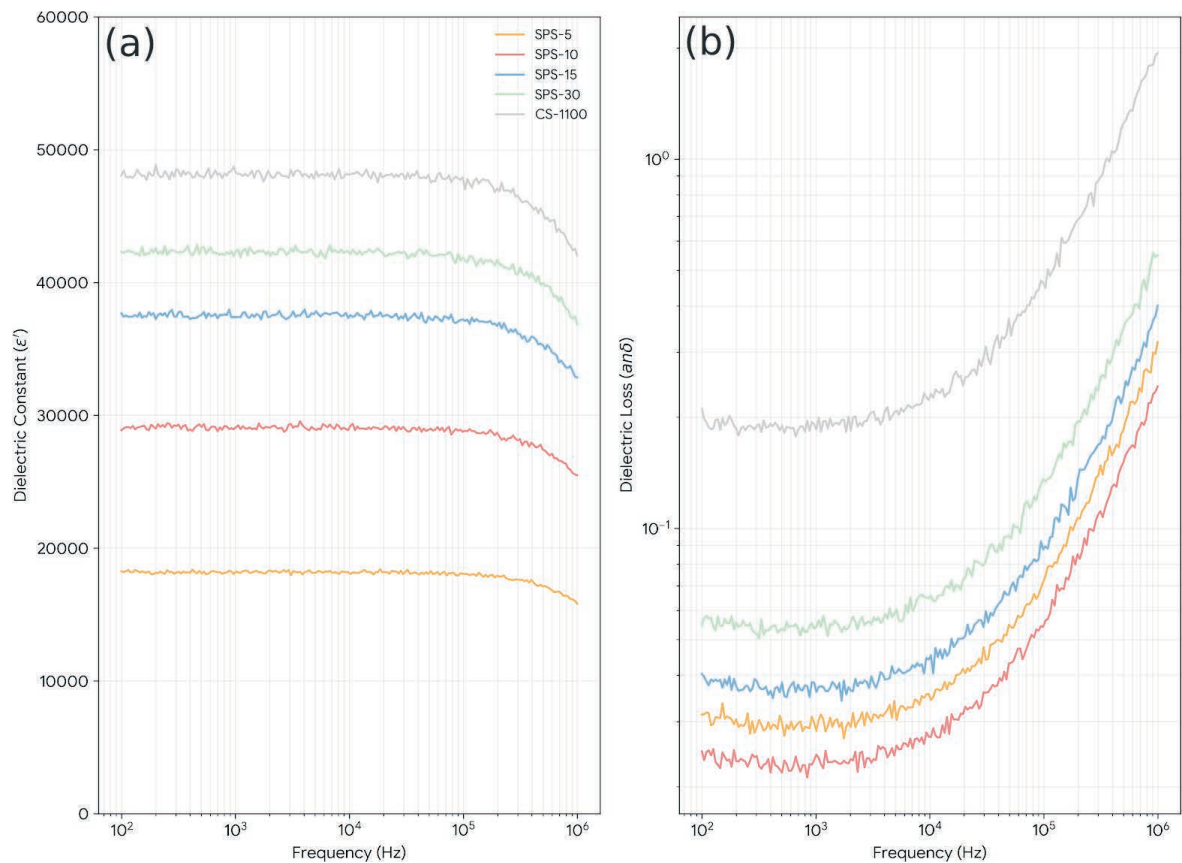


Fig. 6: Frequency dependence of (a) ϵ' and (b) $\tan \delta$ for all CCTO samples measured at room temperature (25 °C).

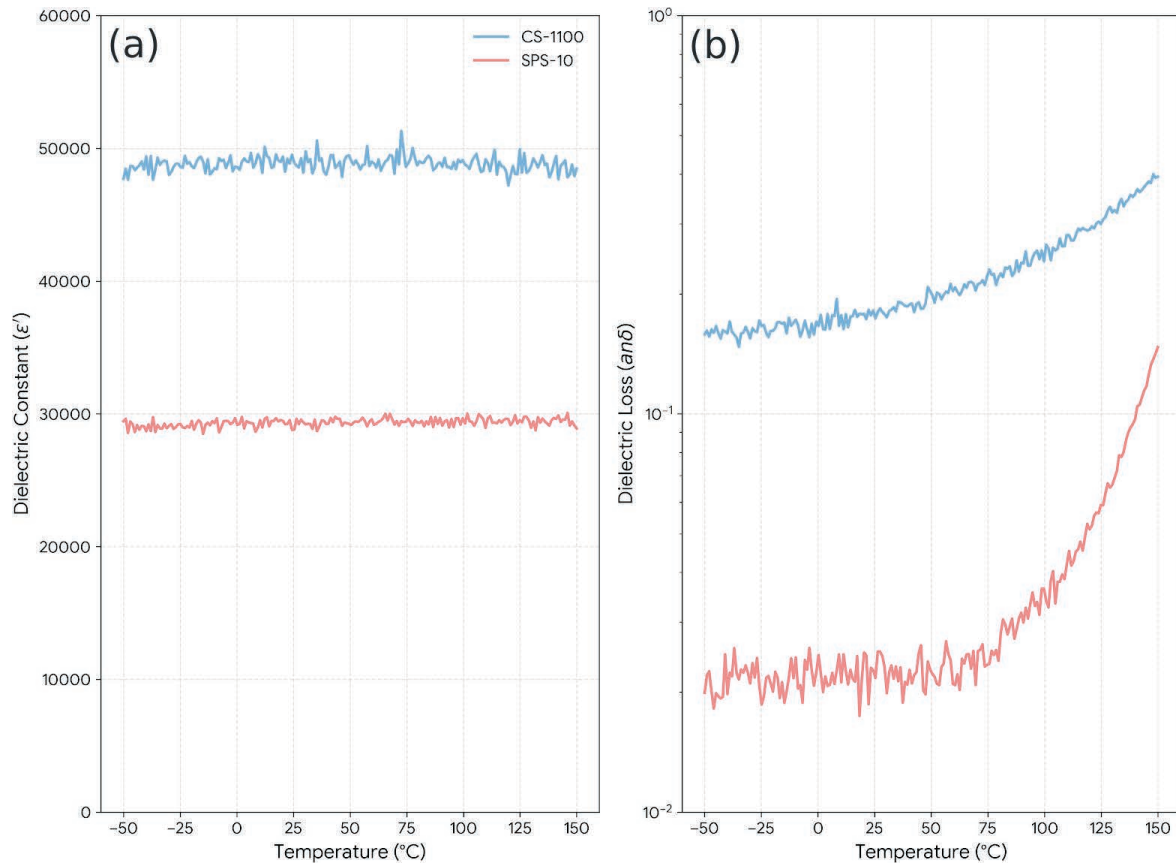


Fig. 7: Temperature dependence of the ϵ' and $\tan \delta$ for the CS-1100 and SPS-10 samples, measured at 1 kHz.

loss reduction. The $\tan \delta$ value at 1 kHz is 0.028 for SPS-5, 0.022 for SPS-10, 0.035 for SPS-15, and 0.051 for SPS-30. The SPS-10 sample combines the lowest dielectric loss with a still high ϵ' of $\sim 29\,000$. The increase in $\tan \delta$ for holding times longer than 10 min is consistent with a progressive departure from the optimally balanced SPS microstructure: grain coarsening becomes more pronounced, the grain-associated resistive term decreases, and defect re-equilibration during the longer dwell may partially restore more conductive pathways within the grains and across imperfect interfaces. Because the available XPS data are surface-sensitive, this latter point is presented as a plausible interpretation rather than as a directly proven defect-chemistry result.

The temperature dependence of the dielectric properties was also investigated for the optimal SPS-10 sample and the CS-1100 sample at a frequency of 1 kHz, as shown in Fig. 7. Both samples exhibit good temperature stability of the ϵ' over a wide temperature range from $-50\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$, which is a characteristic feature of CCTO. However, the dielectric loss behavior is markedly different. The $\tan \delta$ of the CS-1100 sample remains high across the entire temperature range and increases sharply at higher temperatures, indicative of thermally activated conduction processes. The SPS-10 sample, on the other hand, maintains a low $\tan \delta$ (< 0.05) up to approximately $100\text{ }^{\circ}\text{C}$, demonstrating superior thermal stability in its loss characteristics. This enhanced performance at elevated temperatures further underscores the robustness of the grain boundary properties achieved by means of SPS.

(5) Impedance spectroscopy analysis

To separate the electrical contributions of the grains and grain boundaries, complex impedance spectroscopy was performed. Fig. 8 shows the room-temperature Nyquist plots. Within the IBLC framework, CCTO is commonly described by a high-frequency grain-associated response and a low-frequency grain-boundary response^{23,25}. For the CS-1100 sample, the high-frequency intercept on the real axis is small, consistent with a comparatively low grain-associated resistive term. For the SPS samples, the spectra are dominated by the much larger grain-boundary arc. Because the high-frequency contribution is comparatively small and can be affected by parasitic inductive and contact-related artifacts, the fitted bulk-associated term should be interpreted cautiously and mainly in a comparative, rather than absolute, sense.

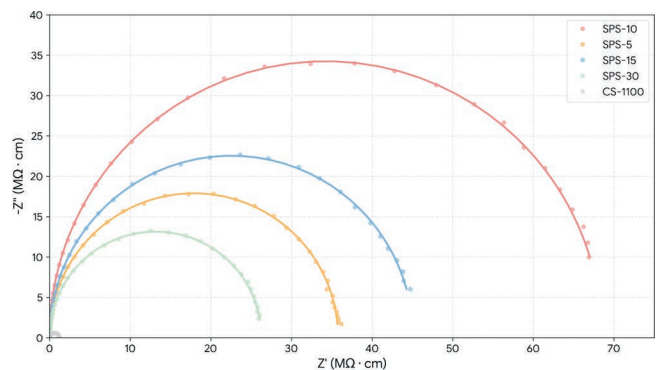


Fig. 8: Nyquist plots of CCTO ceramics at room temperature.

The experimental data were fitted using two RC-type elements in series, representing grain-associated and grain-boundary-associated responses. In the revised manuscript, the fitted values reported in **Table 4** are treated as geometry-normalized parameters. Thus, the quantities previously labeled R_g and R_{gb} are more appropriately discussed as ρ_g and ρ_{gb} -type resistive terms with units of $\Omega \text{ cm}$, rather than as raw resistances. Under this interpretation, the grain-associated parameter is lowest for the CS-1100 sample and higher for the SPS samples, whereas the grain-boundary term increases from 35.8 $\text{M}\Omega\text{-cm}$ for SPS-5 to 68.5 $\text{M}\Omega\text{-cm}$ for SPS-10 before decreasing again at longer dwell times. This trend still tracks the dielectric-loss behavior closely, with SPS-10 showing the largest grain-boundary resistive response and the lowest $\tan \delta$. The capacitance values are likewise reported in geometry-normalized form, so the nF/cm-scale grain-boundary capacitance remains consistent with IBLC-type behavior while avoiding overstatement of the absolute fidelity of the fitted high-frequency intercept.

Table 4: Equivalent circuit fitting parameters obtained from impedance spectroscopy data. The reported resistive and capacitive quantities are geometry-normalized fitting parameters calculated as $\rho = RA/L$ and $C_s = CL/A$, where A is the electrode area and L is the sample thickness.

Sample ID	R_g ($\Omega\text{-cm}$)	C_g (pF/cm)	R_{gb} ($\text{M}\Omega\text{-cm}$)	C_{gb} (nF/cm)
SPS-5	65	110	35.8	2.1
SPS-10	58	105	68.5	3.5
SPS-15	45	102	45.1	4.8
SPS-30	32	98	26.3	5.5
CS-1100	21	125	1.2	8.9

Table 5: Summary of key electrical properties for sintered CCTO ceramics at room temperature (1 kHz for dielectric data).

Sample ID	ϵ' (@1kHz)	$\tan \delta$ (@1kHz)	E_b (V/cm)	α	Φ_B (eV)
SPS-5	18,200	0.028	3150	8.2	0.75
SPS-10	29,100	0.022	5880	12.5	0.89
SPS-15	37,500	0.035	4210	10.1	0.81
SPS-30	42,300	0.051	2950	7.6	0.73
CS-1100	48,100	0.180	450	3.1	0.58

(6) Non-linear electrical properties and potential barrier analysis

The IBLC model, based on back-to-back Schottky-type barriers at grain boundaries, predicts non-linear current-voltage (I-V) characteristics. **Fig. 9** plots current density (J) as a function of the applied electric field (E) for all samples. All ceramics exhibit distinct non-linear

J-E behavior, consistent with previous SPS studies on CCTO³⁵. The breakdown field (E_b), defined here as the field at which $J = 1 \text{ mA/cm}^2$, is much lower for the CS-1100 sample than for the SPS samples. The SPS-10 specimen shows the highest E_b and the largest non-linear coefficient α , indicating the most effective suppression of leakage in the pre-breakdown regime. These trends are consistent with a more favorable barrier configuration in the optimally sintered SPS sample, although the barrier distribution is inferred from the electrical response rather than observed directly.

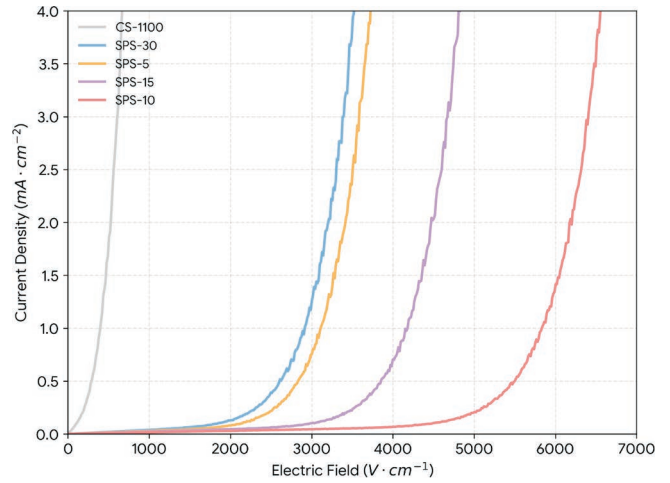


Fig. 9: Current density versus electric field (J-E) characteristics of the CCTO ceramics at room temperature.

The improved non-linear properties and the substantially increased grain-boundary resistive term of the SPS samples suggest that SPS changes the effective interfacial barrier configuration. The apparent barrier height Φ_B was estimated from the pre-breakdown J-E behavior using a Schottky-type thermionic-emission analysis³⁶. By plotting $\ln(J)$ versus $E^{1/2}$, the zero-field current density J_0 was extrapolated and used to calculate Φ_B ⁴. The values summarized in **Fig. 10** and **Table 5** increase from 0.58 eV for the CS-1100 sample to a maximum of 0.89 eV for SPS-10, followed by a decline for SPS-15 and SPS-30. We emphasize that these values should be read as comparative indicators derived within the adopted model, not as direct microscopic measurements of a unique barrier height.

This analysis therefore provides an internally consistent electrical picture rather than a single decisive proof. The trend in Φ_B mirrors the trends in the grain-boundary resistive term, breakdown field, non-linear coefficient, and inverse dielectric loss. Taken together, these results support the view that an intermediate SPS holding time produces the most effective barrier-limited electrical response in the present CCTO ceramics. The revised interpretation is intentionally conservative: the data strongly indicate improved interfacial blocking behavior for SPS-10, but the underlying defect distribution is inferred from the combined structural and electrical evidence rather than assigned to one measurement alone.

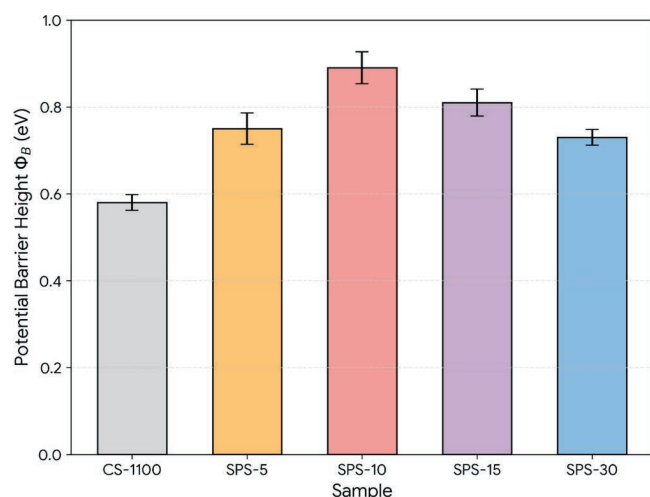


Fig. 10: Calculated grain boundary potential barrier height (Φ_B) for all CCTO samples.

IV. Conclusions

This study demonstrates that Spark Plasma Sintering is an effective route for fabricating $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$ ceramics with simultaneously high ϵ' and substantially reduced dielectric loss. By systematically varying the SPS holding time at 1000 °C, we established clear correlations among densification, grain size, secondary-phase evolution, and electrical response. Compared with the conventionally sintered reference, the SPS ceramics were denser, finer grained, and less affected by secondary-phase residues, while also exhibiting markedly lower $\tan \delta$.

The best overall balance was obtained for the SPS-10 sample, which combined $\epsilon' \approx 2.9 \times 10^4$ with $\tan \delta = 0.022$ at 1 kHz, together with the largest grain-boundary resistive term, the highest breakdown field, and the highest model-derived barrier parameter among the samples studied. TEM revealed cleaner and sharper interfaces in SPS-10 than in the conventionally sintered specimen. Fracture-surface XPS showed comparative differences in Ti and O core-level features, but in the revised interpretation these spectra are used only as supportive near-surface chemical evidence and not as direct proof of grain-boundary-specific vacancy concentrations.

Overall, the revised analysis indicates that the dielectric-loss suppression achieved by SPS arises from the coordinated effects of rapid densification, restrained grain growth, reduced interfacial disorder, and a more favorable effective barrier response. This conclusion is strong at the level of comparative processing-structure-property relationships, even though some microscopic defect details would require additional dedicated characterization in future work. The results therefore provide a practically useful and scientifically cautious basis for further optimization of low-loss CCTO ceramics.

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