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Synthesis, Microstructure, Dielectric Properties, and Insulation Resistance of $SrTiO_3$ Grain Boundary Layer Ceramic Capacitors

W. Bai[1], Y. Zhou[*1], M. Xiao[1], X. Zhao[1], L. Xu[2], H. Xiao[2], Y. Tong[1], C. He[3], J. Pan[3], Q. Xie[3], C. Yang[*1, 2]

[1]School of Materials Science and Engineering, Taiyuan University of Science and Technology, Taiyuan, 030024, China
[2]Faculty of Physics & Electronic Science, Hubei University, Wuhan, 430062, China
[3]Guizhou Zhenhua Electronic Information Industry Technology Research Co. LTD, Guiyang, 550018, China

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Abstract

$SrTiO_3$ grain boundary layer capacitors were prepared by means of a two-step sintering method. The effects of sintering conditions and CuO content in a CuO-PbO-Bi_2O_3-B_2O_3 oxidant on the microstructure, dielectric properties, and insulation resistance of the $SrTiO_3$ capacitors were investigated. The results showed that during semi-conducting sintering, the $SrTiO_3$ grain size increased with increasing sintering temperature, while the porosity decreased and the ceramic became denser. The $SrTiO_3$ capacitor produced at a sintering temperature of 1 420 °C for 2 hours exhibited a maximum dielectric constant of 24 491, a minimum dielectric loss of 0.02 (1 MHz), and a resistance below 0.2 Ω. Furthermore, CuO was used as a partial replacement for PbO during insulating sintering. And the $SrTiO_3$ capacitor achieved optimal performance with a CuO content of 20 wt%, exhibiting a maximum dielectric constant of 26 094, a capacitance temperature coefficient ΔC/C (- 55 °C – 125 °C) ≤ ± 20 %, a dielectric loss below 0.01 (1 MHz), and an average insulation resistance of 90 GΩ (50 V). This research provides a feasible approach to systematically explore the semi-conducting and insulating processes for $SrTiO_3$ grain boundary ceramic capacitors, as well as to develop a low-lead oxidant coating.

Keywords: $SrTiO_3$ ceramics, two-step sintering, dielectric properties, oxidant, insulation resistance value

I. Introduction

With the rapid development of various power systems and modern electronic technology, as well as the trend towards miniaturization and integration of electronic components, the demand for ceramic capacitors with high dielectric performance and high voltage withstand value is increasing [1–4]. $SrTiO_3$, as a new type of multifunctional electronic ceramic material, has become a hot topic in the research of electronic ceramic materials due to its high dielectric constant, low dielectric loss, high voltage withstand strength, and excellent thermal stability [5–6]. $SrTiO_3$ ceramic is a typical ABO_3-type perovskite structure material with a space group of Pm3m and a lattice constant of a = 3.905 [7]. At room temperature, $SrTiO_3$ is considered as a linear dielectric and a paraelectric phase, so its dielectric constant almost does not change with the change of external electric field, which gives it superior voltage stability. In addition, due to the excellent temperature and frequency stability of $SrTiO_3$ over a wide temperature range above the Curie temperature, there is no structural phase transition, making it widely used in electronic, mechanical and functional ceramics fields [8–9].

* Corresponding author: 1042938556@qq.com
co-corresponding author:2013045@tyust.edu.cn

The performance parameters of $SrTiO_3$ grain boundary layer capacitor mainly include dielectric constant, dielectric loss, insulation resistance, and capacitance temperature coefficient. Higher insulation resistance leads to greater withstand voltage of the capacitor, which makes the device less prone to damage and more stable. In recent years, researchers have conducted extensive studies on the effects of semiconductor processing, insulation processing, and insulation oxidizer design on the dielectric performance and insulation resistance of $SrTiO_3$ grain boundary layer capacitor. Fan He *et al.* [10] studied the degradation process of $SrTiO_3$ grain boundary layer capacitor under external electric fields. The degradation mainly manifested as a several-orders-of-magnitude decrease in the insulation resistance of the $SrTiO_3$ grain boundary layer capacitor. Therefore, efforts should be made to prevent such degradation and improve the withstand voltage of the capacitor. Lichen Luo *et al.* [11] studied the fabrication of niobium-doped $SrTiO_3$ ceramics with high dielectric performance under conditions of air and nitrogen atmospheres. Therefore, improving semiconductor processing, insulation processing, and exploring the design of suitable insulation oxidizer components are of great significance for

improving the dielectric performance and insulation resistance of $SrTiO_3$ grain boundary layer capacitors.

The $SrTiO_3$ grain boundary layer capacitor consists of two major components: semiconducting grains and insulating grain boundaries. The semiconducting nature of the grains is achieved by means of donor doping or sintering in a reducing atmosphere, which induces oxygen volatilization and generates oxygen vacancies, resulting in n-type semiconducting grains [12]. The donor doping weakens the Ti-O bond and promotes oxygen volatilization, as shown in Equation 1, where O_O^X represents the oxygen at a normal lattice site, and V_O represents an oxygen vacancy.

$$O_O^X \rightarrow V_O + 2e' + \frac{1}{2}O_2(g) \quad (1)$$

The insulating nature of the grain boundaries can be achieved with two main methods. The first method involves heat treatment in air, which utilizes oxygen diffusion and adsorption in the grain boundaries to form a potential barrier [13]. The second method involves coating the surface of the n-type semiconducting $SrTiO_3$ ceramic with a metal oxide slurry, followed by heat treatment in air, which allows metal ions to diffuse through the grain boundaries into the interior of the $SrTiO_3$ ceramic, resulting in the formation of acceptor surface states and potential barriers [14]. These methods create a potential barrier or a diffusion layer on the n-type semiconducting grain surface to achieve insulating properties at the grain boundaries [15]. During the oxidation heat treatment process, oxygen in the air mainly enters the $SrTiO_3$ semiconductor ceramic through the grain boundaries and diffuses to the grain surface, filling the oxygen vacancies on the grain surface. The decrease in the concentration of oxygen vacancies on the grain surface allows acceptor impurities in the coated oxide slurry to diffuse into the $SrTiO_3$ grain surface, resulting in the formation of a grain boundary insulating layer, as shown in Equation 2.

$$V_O + \frac{1}{2}O_2 \rightarrow O_O^X + 2P \quad (2)$$

In the insulation process of $SrTiO_3$ grain boundary layer capacitor ceramics, the prevalent practice involves the use of insulating oxides predominantly containing PbO. This selection is rooted in the substantial advantages associated with Pb-based oxides, including the augmentation of the ceramic's dielectric constant, thus enhancing its charge storage capability and, consequently, bolstering the performance of capacitors. Furthermore, Pb-containing oxides contribute to the enhancement of temperature stability in electronic ceramics, a vital requirement for applications demanding consistent performance across a wide temperature spectrum [16]. Nonetheless, it is paramount to emphasize that lead is a toxic substance, thereby underscoring the inherent environmental and human health risks entailed in the utilization of lead-based oxide additives. Currently, the lack of lead-free ceramic capacitors with high dielectric performance, including low electric field strength and small maximum polarization, has hindered the development of electronic components toward miniaturization and integration. Hence, the partial substitution of CuO for PbO within insulating oxides not only aligns with environmental regulations and market demands but also holds the potential to facilitate the development of insulating phases within the grain boundaries of $SrTiO_3$ ceramics, thus further enhancing their insulation resistance.

This study employed a two-step sintering method to prepare $SrTiO_3$ grain boundary capacitors, and systematically investigated the effects of different sintering conditions and CuO contents in CuO-PbO-Bi_2O_3-B_2O_3 oxidizers on the microstructure, grain size, dielectric properties, and insulation resistance of the $SrTiO_3$ grain boundary capacitors. The aim was to explore an optimal process for semiconducting and insulating $SrTiO_3$ grain boundary ceramic capacitors. Additionally, this research aimed to develop oxidizer coatings with lower lead content to enhance their dielectric properties and insulation resistance, in order to meet the demands of miniaturization and integration in electronic devices.

II. Experimental

$SrTiO_3$ grain boundary layer capacitor was prepared with a two-step sintering method. $SrCO_3$ (> 99 %) and TiO_2 (> 99 %) were ball-milled in ethanol for 24 hours, and the resulting slurry was dried and sintered at 1 150 °C for 2 hours to obtain $SrTiO_3$ powder. The powder was then rolled into a thin sheet and subjected to a gel removal treatment at 600 °C for 0.5 hours, prior to being placed in a tube furnace and exposed to a reducing gas mixture of N_2 and H_2 at a certain proportion. The semiconducting sintering process was conducted in the temperature range from 1 380 °C to 1 460 °C for 1 to 5 hours. After the first semi-conducting sintering, an oxidizer was prepared in accordance with the proportions of 35 wt% Bi_2O_3, (55-x) wt% PbO, 10 wt% B_2O_3, and x wt% CuO. This oxidizer was blended with n-butyl carbitol solvent in specified ratios and subjected to a ball milling procedure. Subsequently, the prepared slurry was applied to semiconducting STO ceramic substrates using a dual-sided spin-coating technique, resulting in an oxide slurry thickness of approximately 8 – 12 μm. Subsequent insulation sintering was performed at 1 160 °C for 1 to 5 hours. Finally, the insulation $SrTiO_3$ ceramic substrate was printed with silver electrodes, and thermally treated at 600 °C for 0.5 hours.

The microstructure of the samples was observed with scanning electron microscopy (SEM, JSM-7100F, JEOL, Japan), and the dielectric parameters and insulation resistance were measured using a spectrum analyzer (IM3590, HIOKI, Japan) and an insulation resistance tester (TH2681, Changzhou Tonghui Electronics Co., Ltd, China), respectively. These experimental steps and measurements constitute a comprehensive method for synthesizing and characterizing $SrTiO_3$ ceramic capacitors.

III. Results and Discussion

SEM images of $SrTiO_3$ ceramic samples obtained after the first-step sintering process are presented in Fig. 1, which reflects the effects of different sintering temperatures on the crystallization and phase formation of $SrTiO_3$ for the same sintering time (2 h). It can be observed

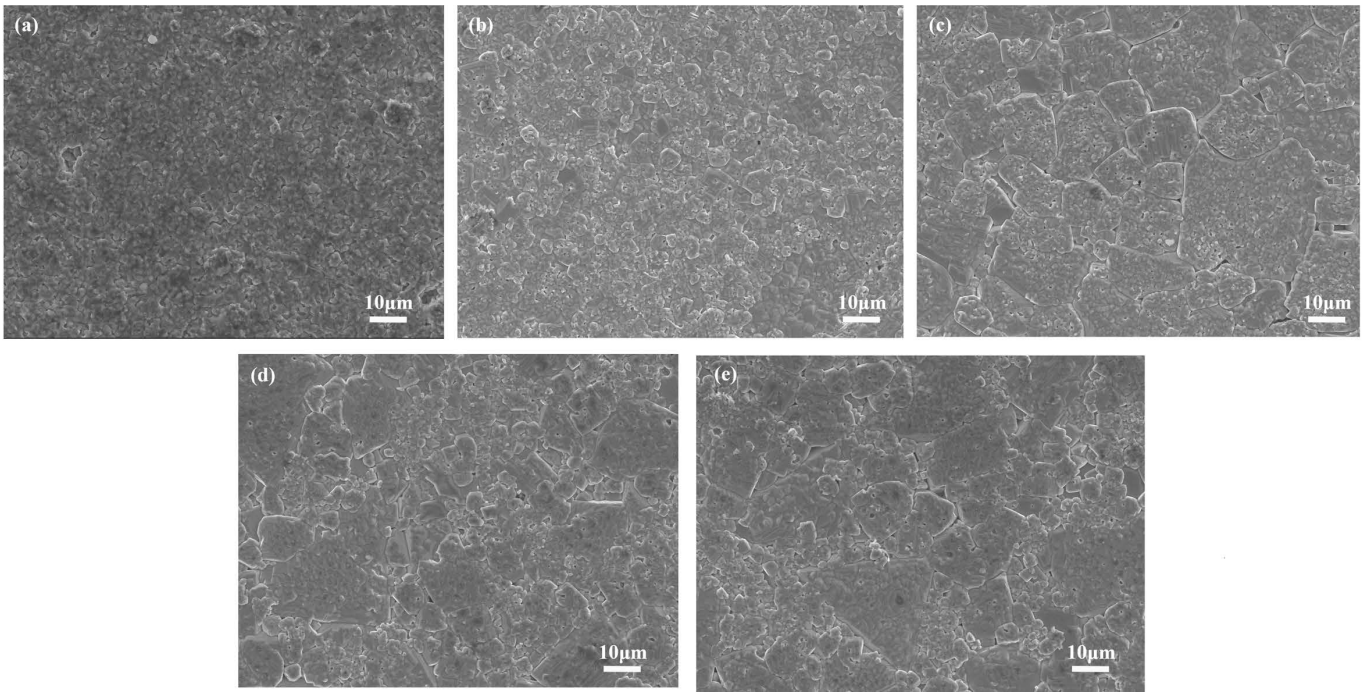

Fig. 1: SEM images of semiconducting samples obtained by secondary sintering at different temperatures.

from Fig. 1 that when the sintering temperature is relatively low at 1 380 °C (Fig. 1a), the sample appears as powder with fine particles and no obvious grain boundary. It indicates that the sintering of $SrTiO_3$ sample is incomplete at this temperature. As the sintering temperature increases to 1 400 °C (Fig. 1b), $SrTiO_3$ sample still exists as fine particles, and the sintering remains incomplete. However, compared with the 1 380 °C case, the gaps between particles decrease, and the ceramic plate becomes denser. As the sintering temperature is raised to 1 420 °C (Fig. 1c), the presence of pores is reduced, and the ceramic plate becomes more compact, with large grains appearing that are much larger than the original powder particles. Further increases in sintering temperature to 1 440 °C (Fig. 1d) and 1 460 °C (Fig. 1e) result in complete sintering of $SrTiO_3$, with the pores disappearing, and the samples becoming highly dense, consisting almost entirely of grains that are significantly larger than the original powder particles. The above analysis indicates that the sintering process and grain growth of $SrTiO_3$ ceramics are highly sensitive to sintering temperature. Therefore, samples with different microstructures can be obtained by adjusting the sintering temperature during the first-step sintering process.

Fig. 2(a) and (b) depict the changes in the dielectric constant and dielectric loss of $SrTiO_3$ samples at different sintering temperatures as a function of measurement frequency. The dielectric constant decreases with increasing frequency within a certain range, while the dielectric loss first decreases and then slowly increases with frequency. These features of the dielectric constant and loss may be related to the microstructure of the material. As previously analyzed by means of SEM, the microstructure of the samples sintered at different temperatures is different, which may affect the dielectric properties of the material. Fig. 2 indicates that when the sintering temperature of the semiconductor is low (< 1 400 °C) and the sintering is insufficient, the dielectric constant of $SrTiO_3$ decreases significantly with increasing test frequency. When sintered at 1 380 °C, the dielectric constant of the sample is the smallest at $\varepsilon_r = 6\,000$.

This is because the number of pores in the ceramics increases as the sintering temperature decreases. When the sintering temperature is relatively low, there are more pores on the grains and the incomplete grain boundaries lead to a relatively low dielectric constant. This result is consistent with the SEM results, which show that $SrTiO_3$ has incomplete grains and indistinct grain boundaries. However, when the sintering temperature is high (> 1 420 °C) and $SrTiO_3$ is fully sintered to form dense grains, the dielectric constant of the sample remains constant and does not change significantly with measurement frequency, indicating that the grain boundary capacitors of $SrTiO_3$ exhibit good frequency stability. The results show that the sintering temperature of the semiconductor has a significant effect on the dielectric constant of $SrTiO_3$, but the relationship is not monotonic. When the semiconductor is sintered at 1 420 °C, the dielectric constant of $SrTiO_3$ reaches the maximum of 18 000 and the minimum dielectric loss is 0.015. In addition, Fig. 2(b) shows that, similar to the dielectric constant, the dielectric loss of $SrTiO_3$ also exhibits good frequency stability, with a low dielectric loss of less than 0.05 at high frequencies and some even lower than 0.01, indicating that $SrTiO_3$ has extremely low dielectric loss and is suitable for application in high frequency or microwave fields.

We conducted an in-depth investigation into the effect of the semiconductor sintering time on the crystallization and phase formation of $SrTiO_3$ ceramics. During the experiment, we maintained the sintering temperature at a constant 1 420 °C, and varied the sintering time from 1 to 5 hours. The results, as shown in Fig. 3, reveal that

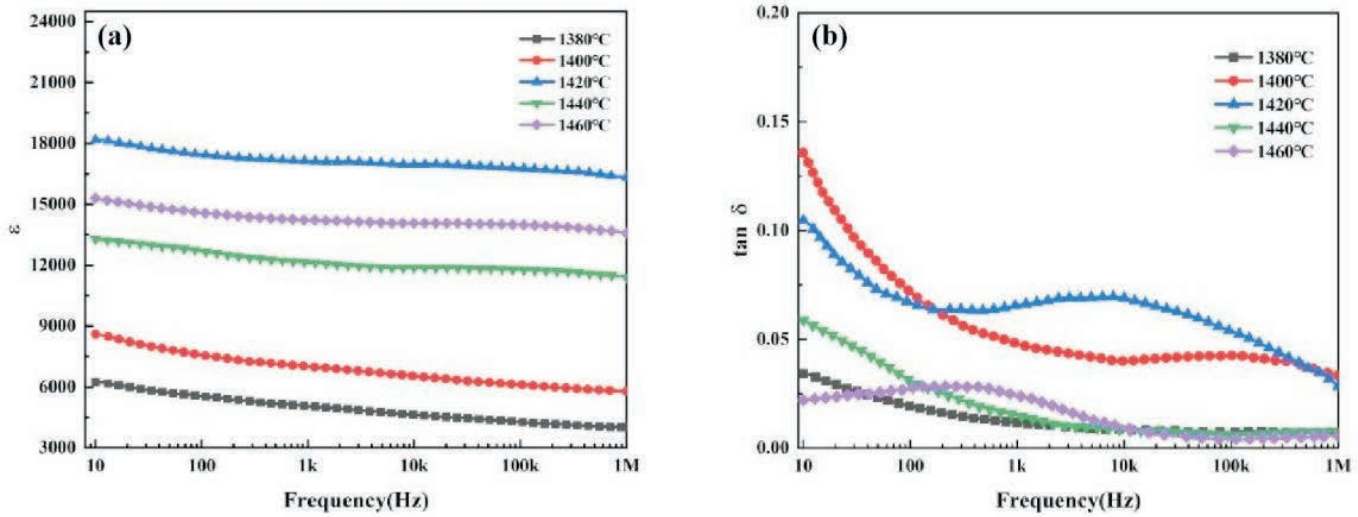

Fig. 2: The dielectric properties of samples sintered at different temperatures.

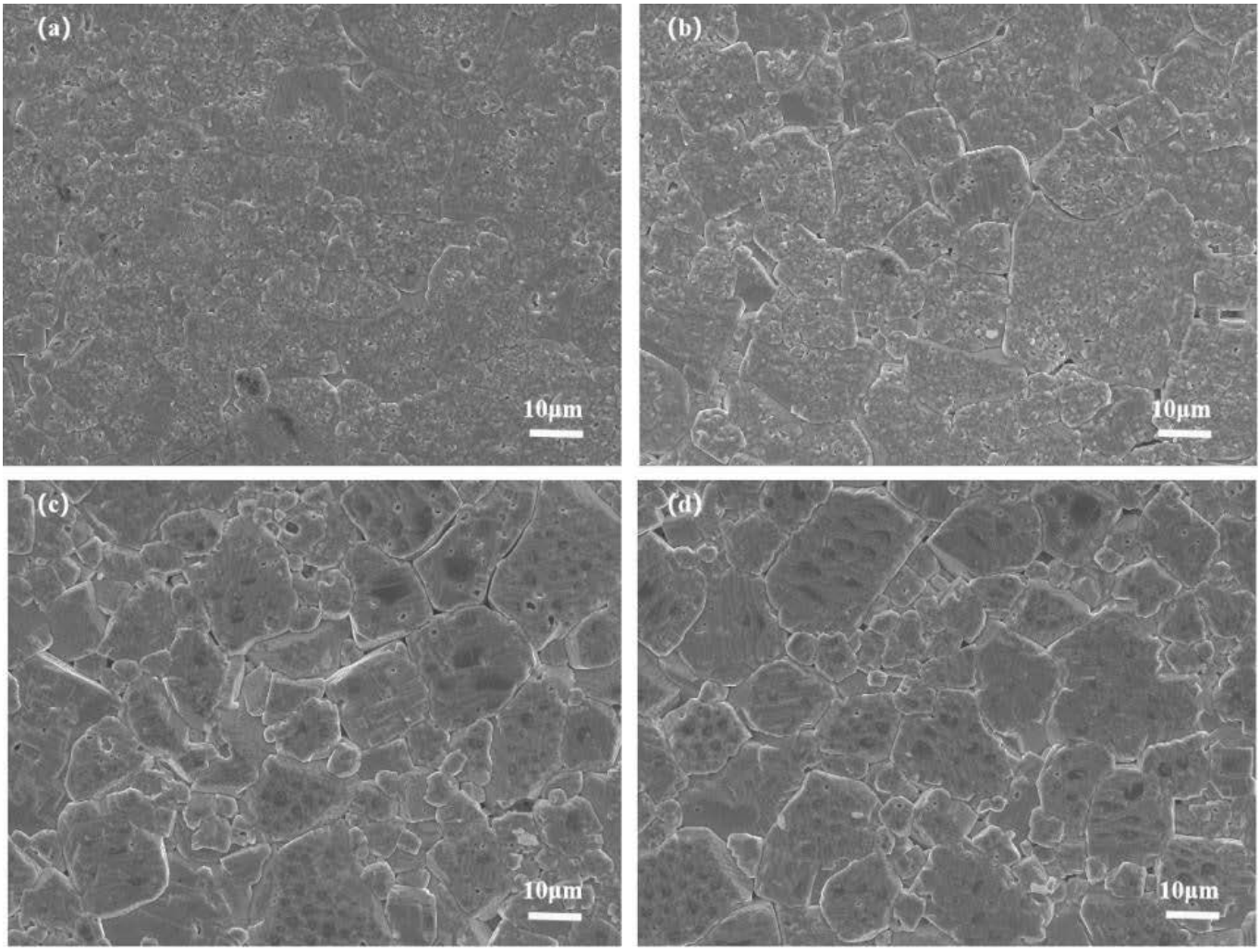

Fig. 3: Microscopic morphology of $SrTiO_3$ ceramic samples subjected to different heat treatment times.

regardless of the sintering time, $SrTiO_3$ ceramics can achieve crystallization and phase formation. However, when the holding time is only 1 hour, numerous small particles appear on the surface of the sample, the grain boundaries are indistinct, and pores exist between the grains, indicating insufficient sintering of $SrTiO_3$ at this time. As the holding time increases to 2, 3, and 5 hours, the number of particles and pores between the particles

on the sample surface decreases, the grain size gradually increases, the grain boundaries become clearer, and the sintering is complete, forming dense $SrTiO_3$ grains.

Fig. 4(a) and (b) show the dielectric constant and loss spectra of $SrTiO_3$ ceramic, respectively. They reflect the influence of different annealing times on the dielectric properties of $SrTiO_3$ ceramic at the same semiconductor temperature (1 420 °C). As analyzed above, the dielectric constant of $SrTiO_3$ ceramic is affected by the size of its grains and the number of pores. The larger the grains and the fewer the pores, the lower the dielectric constant, and vice versa. Upon further analysis of the graphs, it can be observed that when the annealing time is 2 hours, the grain size and number of pores of $SrTiO_3$ ceramic follow the above rule, and it exhibits optimal dielectric properties at high frequency. Specifically, the dielectric constant and loss are 24 491 and 0.015 (1 MHz), respectively. Therefore, annealing at 1 420 °C for 2 hours is the optimal condition for semiconductor processing, as it results in the best dielectric properties due to its dense structure. Additionally, Fig. 4 exhibits an intriguing phenomenon, wherein the increase in sintering duration from 2 hours to 5 hours is associated with a reduction in the number of pores between particles, while the dielectric constant initially decreases and subsequently increases. This constitutes a pivotal observation that delves into the intricate relationship between crystal defects and dielectric performance. We posit that this phenomenon can be elucidated through the prism of crystal defects and the rearrangement processes. When the sintering time is extended from 2 h to 3 h, excessive sintering may engender an augmentation of point defects and lattice defects within the crystal. These defects, to a certain extent, can attenuate the dielectric constant. However, when the sintering time is extended from 3 h to 5 h, the crystal may undergo a rearrangement or restorative process, thereby diminishing the tally of point defects and lattice defects and ameliorating the structural integrity of the crystal, consequently engendering an augmentation in the dielectric constant, as observed in Fig. 4.

The dielectric properties of $SrTiO_3$ grain boundary capacitors are determined by both the grains and grain boundaries [17–18]. During the semiconducting process, sintering is carried out in vacuum or in a reducing N_2/H_2 gas mixture, which leads to the generation of a large number of oxygen vacancies in $SrTiO_3$ grains, transforming them from insulators into N-type semiconductors with good conductivity. The first step of semiconducting sintering determines the grain size, distribution, and conductivity of $SrTiO_3$ [19–20]. In addition to the important influence of grains on the electrical properties of $SrTiO_3$ grain boundary capacitors, the grain boundaries also have a decisive impact on the dielectric properties of the capacitor [21]. In theory, the thinner the diffusion layer connected to the grain boundary, the smaller the dielectric loss of the $SrTiO_3$ grain boundary capacitor [22]. At the same time, the insulation resistance as well as the capacitance values of $SrTiO_3$ grain boundary capacitor are also determined by the structure and properties of the grain boundaries [23].

Therefore, in the fabrication process of $SrTiO_3$ grain boundary layer capacitors, the second step of insulation sintering is not only essential but also more important. Generally, the process of insulation sintering after semiconducting is to first coat the surface of the $SrTiO_3$ ceramic with a layer of metal oxide as an oxidant and then sinter at a temperature slightly lower than that of semiconducting. $PbO\text{-}Bi_2O_3\text{-}B_2O_3$ is the most common oxidant in scientific research and industrial production, where ions such as Pb^{2+}, Bi^{3+}, and B^{3+} diffuse from the surface to the $SrTiO_3$ grain boundary by thermal diffusion [24]. Pb^{2+} acts as an acceptor and forms a potential barrier resistance with positively charged oxygen vacancies to create a space charge region. Bi^{3+} has a strong adsorption effect on O atoms, which is conducive to the entry of oxygen in the air into the grain boundary and grain to insulate $SrTiO_3$ grain boundary layer capacitors. B^{3+} forms a glassy substance with Bi^{3+}, Pb^{2+}, O^{2-} ions at the grain boundary and further enhances the insulation resistance of $SrTiO_3$ grain boundary layer capacitors. However, $PbO\text{-}Bi_2O_3\text{-}B_2O_3$ oxidants contain a high concentration of lead, which can cause great harm to the environment and human health [25]. Therefore, in order to reduce the lead content in the oxidant and improve the comprehensive electrical properties of $SrTiO_3$ grain boundary layer capacitors, we partially replaced PbO with CuO and studied the influence of $CuO\text{-}PbO\text{-}Bi_2O_3\text{-}B_2O_3$ quaternary oxidants on the dielectric properties of $SrTiO_3$ grain boundary layer capacitors.

The spectra of dielectric constant with different CuO contents, using $CuO\text{-}PbO\text{-}Bi_2O_3\text{-}B_2O_3$ quaternary oxide, are shown in Fig. 5(a) and (b). The semiconducting conditions of $SrTiO_3$ were 1 420 °C for 2 hours, and the insulation conditions were 1 060 °C for 0.5 hours. Fig. 5(a) shows that CuO substitution has a significant enhancing effect on the dielectric constant of $SrTiO_3$ grain boundary layer capacitors. When the CuO content increases from 10 wt% to 15 wt%, the introduction of additional point defects and lattice defects in the material leads to a non-uniform charge distribution, thus diminishing the dielectric constant. However, when the CuO content increases from 15 wt% to 20 wt%, it is plausible that a rearrangement or repair process occurs within the crystal, which can reduce the number of point defects, rectify lattice defects, and enhance the structural integrity of the crystal, thereby increasing the dielectric constant. Finally, as the CuO content rises to 25 wt%, this process may introduce an excessive amount of CuO, resulting in structural disarray within the crystal and the emergence of new defects, once again reducing the dielectric constant. And when the CuO content is 20 wt%, the dielectric constant of $SrTiO_3$ grain boundary layer capacitor reaches the maximum value of 26 094, which is 44.97 % higher than that without coating, which was 18 000. Fig. 5(b) shows the effect of the $CuO\text{-}PbO\text{-}Bi_2O_3\text{-}B_2O_3$ quaternary oxide on the dielectric loss of $SrTiO_3$ grain boundary layer capacitors. When the CuO content reaches 20 wt%, the $SrTiO_3$ grain boundary layer capacitor exhibits a maximum dielectric loss of 0.006 at a frequency of 1 MHz, which is less than half of the dielectric loss value of 0.015 observed in the uncoated condition depicted in Fig. 4(b).

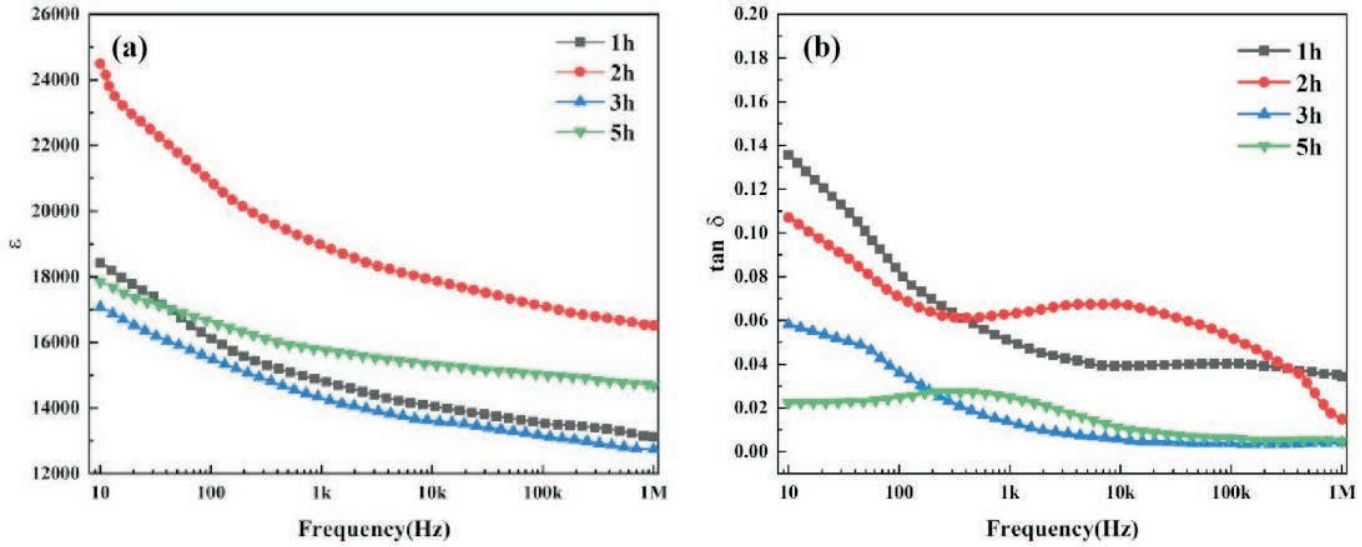

Fig. 4: The dielectric properties of $SrTiO_3$ ceramic samples subjected to different heat treatment times.

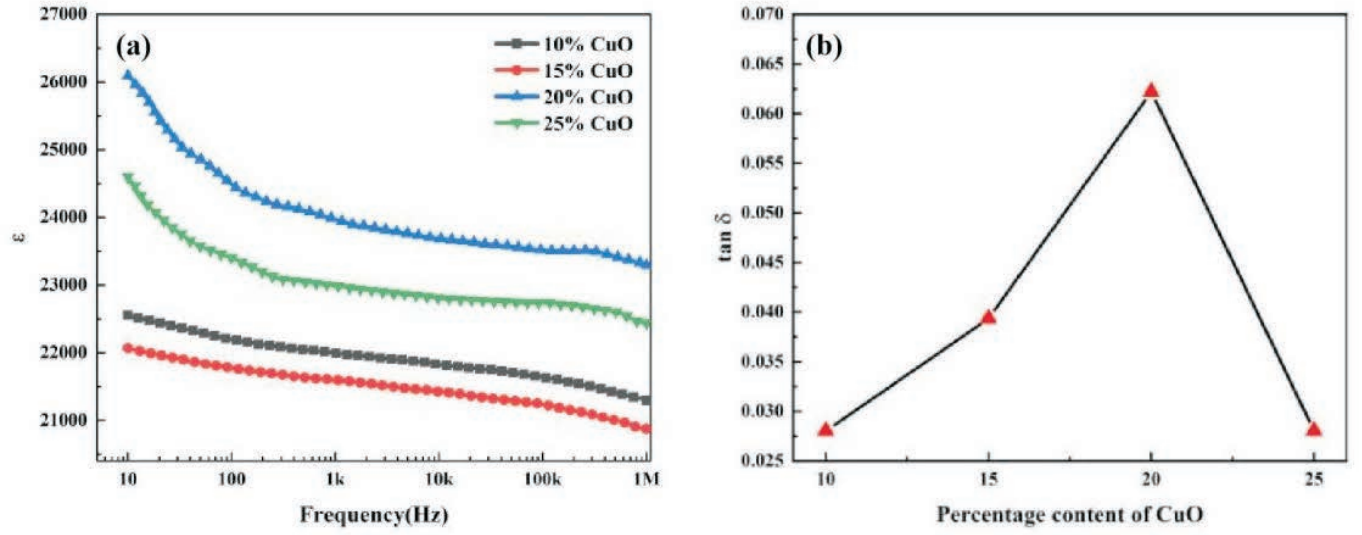

Fig. 5: The dielectric properties of samples insulated after different proportions of CuO oxidant.

Fig. 6 shows the influence of the quaternary oxidant CuO-PbO-Bi_2O_3-B_2O_3 and CuO content on the insulation resistance and capacitance temperature coefficient of the $SrTiO_3$ grain boundary layer capacitor. In order to reduce accidental errors and increase the credibility of the conclusions, multiple samples were repeatedly measured in this experiment to enhance statistical significance. From Fig. 6, it can be seen that using CuO-PbO-Bi_2O_3-B_2O_3 quaternary oxidant, the $SrTiO_3$ grain boundary layer capacitors' insulation resistance (50 V) exceeds 1 GΩ, which belongs to high insulation resistance grain boundary layer capacitor. When the CuO content is 20 wt%, its insulation resistance value is the highest, with a mean value of 90 GΩ. The reason why it can achieve better insulation effect is that in the semiconductive ceramic $SrTiO_3$, impurity Cu has the property of acceptor, which will form trapping centers for conducting electrons near the grain boundaries [26–27]. In addition, as shown in Equation (3), the oxygen activity released by CuO decomposition is very strong, which makes an important contribution to the re-oxidation of the grain boundaries and the formation of diffusion compensation layer.

$$CuO \rightarrow 2Cu_2O + O_2 \uparrow \quad (3)$$

Therefore, CuO is an oxidant that can significantly increase the $SrTiO_3$ insulation resistance. And the reason why the CuO-PbO-Bi_2O_3-B_2O_3 four-element oxide coating can obtain $SrTiO_3$ grain boundary ceramic capacitor samples with better comprehensive performance is that this oxide coating combines the advantages of CuO and PbO-Bi_2O_3-B_2O_3 coatings. However, when the CuO content reaches 25 wt%, it may lead to its redistribution within the material, giving rise to lattice distortions, impurities, interfaces, or other defects. These effects are likely to result in electron scattering or the promotion of electron transitions, leading to a reduction in insulation resistance. Moreover, an excessive CuO content may lead to an overabundance of electron tunneling, further diminishing its insulation resistance.

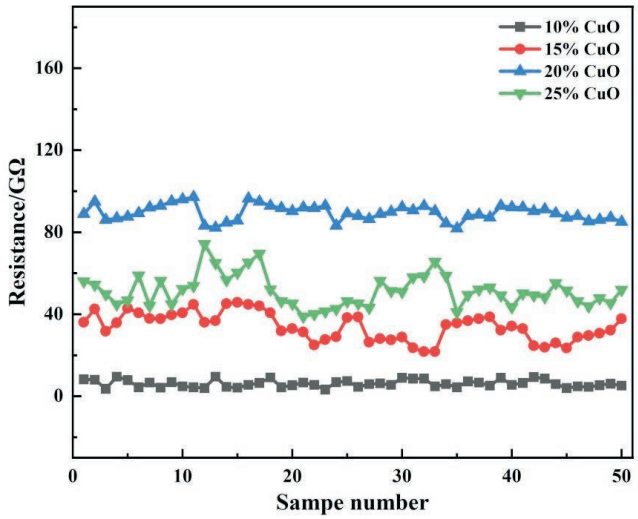

Fig. 6: The insulation resistance of samples insulated using different proportions of CuO oxidant.

Fig. 7 shows the capacitance temperature coefficient characteristics of $SrTiO_3$ grain boundary layer capacitors. Using the capacitance at room temperature (25 °C) as a reference, it can be seen from the graph that the capacitance temperature coefficient ΔC/C reaches its minimum value in the temperature range of −55 °C to 125 °C when the CuO content is 20 wt%. The stability of the capacitor is the best, meeting industrial application conditions, i.e., ΔC/C ≤ ±20 %. The reason why the CuO-PbO-Bi_2O_3-B_2O_3 four-element oxide coating can obtain $SrTiO_3$ grain boundary ceramic capacitor samples with better comprehensive performance is that this oxide coating combines the advantages of CuO and PbO-Bi_2O_3-B_2O_3 coatings. It can not only form a good liquid phase at a low temperature, penetrate continuously along the grain boundary, and form an amorphous insulating second phase at the grain boundary, but also promote the uniform distribution of CuO in the grain boundary, fully exerting its favorable effect on forming the grain surface diffusion compensation layer, thereby improving the insulation effect of the grain boundary.

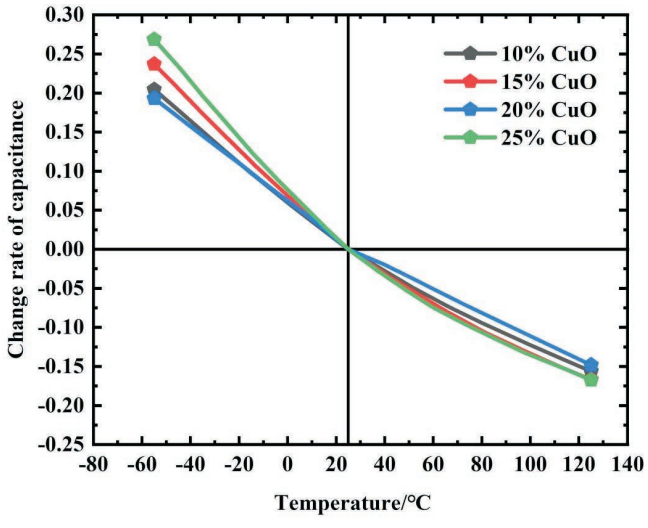

Fig. 7: Temperature coefficient of capacitance testing on spin-coated samples with different proportions of CuO oxidant.

IV. Conclusions

The aim of this study was to systematically explore the optimal processing conditions for semiconductivization and insulation during the preparation of $SrTiO_3$ grain boundary layer ceramic capacitors, and to investigate the effect of CuO content in a quaternary oxide mixture of CuO-PbO-Bi_2O_3-B_2O_3 on the dielectric properties, insulation resistance, and capacitance temperature coefficient of the grain boundary layer capacitors. The results showed that when the semiconductivization conditions were 1 420 °C×2 h, the $SrTiO_3$ semiconductivized ceramic capacitor was fully sintered and had the best dielectric performance. When the CuO content in the CuO-PbO-Bi_2O_3-B_2O_3 quaternary oxide mixture was 20 wt% and the $SrTiO_3$ ceramic capacitor was insulated using this mixture, the dielectric constant and dissipation factor of the sample were 26 000 and 0.008 (1 MHz), respectively, while the insulation resistance was 90 GΩ (50 V). The capacitance temperature coefficient of the sample was in the minimum value state in the temperature range of −55 °C to 125 °C, and the stability met the industrial application conditions, that is, ΔC/C ≤ ±20 %. This suggests that CuO, as a substitution for the acceptor oxide PbO, can effectively enhance the insulation performance of the sample. Therefore, by using the optimal processing conditions for semiconductivization and insulation explored in this study and by using the CuO-PbO-Bi_2O_3-B_2O_3 quaternary oxide mixture developed for insulation coating of the sample, grain boundary layer ceramic capacitors with better comprehensive performance indicators can be obtained, which meet the development needs of miniaturization, integration, and environmental protection of electronic components and can be used in industrial applications.

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