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A 10 MHz to 80 GHz Low-Temperature Cofired Ceramic Ball Grid Array Board-to-Interposer Transition for Chip Scale Packages

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Abstract

Presented here are the design, fabrication, and measurement results of a low-temperature cofired ceramic (LTCC) board-to-interposer transition utilizing a flip-chip ball grid array (BGA) interconnect that provides excellent electrical performance up to and including 80 GHz. A test board is fabricated in LTCC and another smaller LTCC part is used as an interposer for demonstration purposes. This BGA board-to-interposer interconnect is designed as a back-to-back pair of transitions with an assembly consisting of an LTCC interposer, an LTCC motherboard, and a BGA interconnect constructed with 260-μm-diameter polymer core solder balls. The LTCC material employed is DuPont™ GreenTape™ 9K7. Full-wave simulation results predict excellent electrical performance from 10 MHz to 80 GHz, with the board-to-interposer BGA transition having less than 0.5 dB insertion loss at 60 GHz and less than 1 dB insertion loss up to 80 GHz. In an assembled package (back-to-back BGA transitions), the insertion loss was measured to be 1 dB per transition at 60 GHz and less than 2 dB per transition for all frequencies up to 80 GHz.

Keywords: LTCC, BGA interconnect, chip scale package, millimeter-wave, transition

I. Introduction

The high level of integration in today's system-in-package (SiP) millimeter-wave applications requires high-performance interconnect designs that minimize electrical loss, provide good reliability, and minimize cost. Standard industry practice to meet these requirements typically involves solder balls arranged in a ball grid array (BGA) [1]. Low-temperature cofired ceramic (LTCC) packages are an excellent choice for many SiP applications owing to a very close Coefficient of Thermal Expansion (CTE) match to semiconductor materials and its multilayer capability supporting features such as vertical radio frequency (RF) and microwave transitions, making complex routing of controlled impedance transmission lines easier. One of the more challenging packaging issues today is to realize a high-volume vertical interconnect that can function up to 80 GHz with conventional 250 – 300-μm-diameter solder balls.

Several authors have published work on such BGA interconnect designs in recent years. Staiculescu *et al.* published their study of a BGA interconnect from a Duroid board to an LTCC package [2]. They used 254-μm solder balls and showed results up to 12 GHz. Liang *et al.* presented a BGA package with an alumina substrate and 280-μm solder balls [3]. They claim that a single transition including the solder balls, vertical vias, and a short length of coplanar waveguide (CPW) on the package offered an insertion loss of 0.3 dB out to 36 GHz. Kangasvieri *et al.* published a vertical interconnect from LTCC motherboard to LTCC package which featured a cascade of a BGA transition followed by in internal via transition from the bottom the top of the package [4]. They used 300-μm solder balls and achieved an insertion loss of 1 dB or better up to about 66 GHz.

The board-to-interposer BGA transition described in this paper is, to the best of our knowledge, the broadest bandwidth BGA transition published to date with demonstrated bandwidth up to 80 GHz. The transition features 260-μm solder balls in the BGA arranged in a configuration to guarantee controlled impedance performance over a wide frequency bandwidth. The transition has a measured insertion loss of 2 dB or better up to 80 GHz and a return loss of 10 dB or better for almost all frequencies up to 80 GHz. This transition is well suited for both 60 GHz and 77 GHz chip scale packages.

II. Transition Design

The 3D cutaway view shown in Fig. 1 showcases the basic metal features of this millimeter-wave BGA transition. The test board contains a nominal 50Ω grounded coplanar waveguide (GCPW) that provides ground-signal-ground (GSG) microprobe access at one end and is connected to the signal solder ball at the other. The top of the signal solder ball is connected to a signal catch pad and signal via connecting to a 50Ω stripline inside of the package. The

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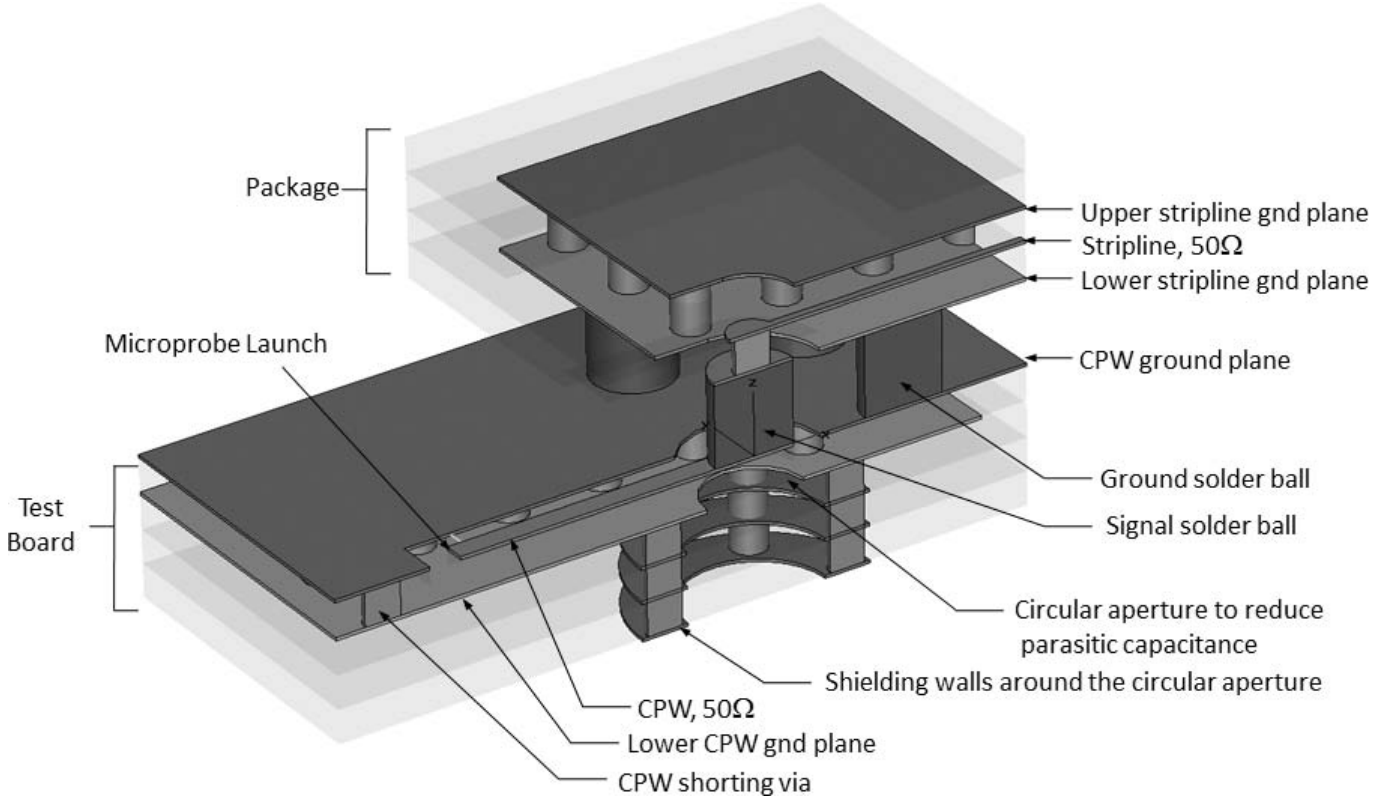

Fig. 1 : 3D cutaway view along the line of symmetry labeling features of the BGA transition.

signal path inside of the test board and the package is represented in orange and ground planes are shown in red and light green. Solder balls are shown in dark green, including the signal solder ball connecting the signal traces from the test board to the package. Ground vias are shown in pink in the package and test board. A cutoff mode circular waveguide is shown below the aperture.

Both the test board and the package were fabricated using DuPont™ GreenTape™ 9K7 LTCC tape with a nominal green state thickness of 5 mils and a post-fired thickness of approximately 4.25 mils (108 μm). The design of both the test board and the package contained four dielectric layers. The 9K7 dielectric was modeled based on extensive material characterization with a dielectric constant of ε_r = 7.0 and a loss tangent of 0.0012 at 60 GHz. All metallizations in the designs were gold thick-film conductors from the 9K7 suite of materials. Metal thickness is simulated at 10 μm. All metal elements (excluding the solder balls) in the simulation are assigned a conductivity of 3.3E7 S/m. Therefore the simulated effective surface resistance of metal layers is approximately 3 mΩ/sq. Solder balls have a defined conductivity of 5.0E5 S/m. All vias are nominally 5 mils in diameter in the green state and 4.56 mils (116 μm) in diameter post fired. Grounding vias have a minimum center-to-center pitch of 12 mils on each side of the board CPW line and the package stripline. Solder balls are assumed to have polymer cores, and they are modeled as 260-μm-diameter cylinders of height 260 μm to account for the solder fillets. The board area occupied by this BGA transition is approximately 2.0 mm x 2.3 mm.

An ultraviolet (UV) laser ablation process was used in the manufacturing process to achieve fine features of the GCPW trace on the test board and the stripline, signal catch pad, and antipad in the package [5]. Laser ablation realizes smaller lines and spaces when compared to industry standard screen-printing by enabling minimum gap dimensions that can be nearly as small as the laser diameter. The UV laser used during the fabrication of these test parts had a focused laser beam diameter of 20 μm. Critical features that required laser ablation included the GCPW gap of 60 μm and the stripline width of 50 μm. The simulations took into account the removal of dielectric created by the laser ablation process by including a 50-μm-deep trench around features that were fired in the post-fired state. These air-filled trenches are responsible for reducing the parasitic capacitance around signal pads associated with the signal solder ball and also help to lower the insertion loss of the CPW structure.

Details of the solder ball layout and the interposer GCPW are shown in Fig. 2. The GCPW (shown in orange) has a width of 135 μm and a gap of 60 μm with grounding vias (pink) to each side of the trace. In the transverse direction, ground solder balls (shown in green) are located 600 μm center-to-center away from the signal solder ball. A row of three ground solder balls is located 500 μm center-to-center away from the signal solder ball in the longitudinal direction, with the middle ground solder ball centered with the signal solder ball. These three ground solder balls are spaced 500 μm apart center-to-center in the transverse direction. Each solder ball has its own catch pad printed on the surface of the test board. The solder ball catch pads are formed with a solderable screen-printed gold conductor, surrounded by a solder dam (not shown in figure) created with a dielectric solder mask print, and each measure 260 μm in diameter.

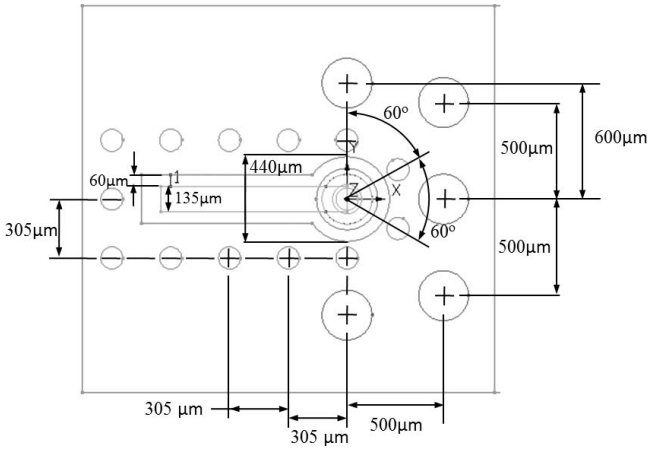

Fig. 2: Dimensions of solder ball layout and board layout.

Several key features in the design enable such high performance up to 80 GHz. The first such feature is a circular aperture formed in the lower CPW ground plane of the test board, directly below the CPW signal pad and the signal solder ball. This aperture, which was inspired by a similar feature suggested by Kangasvieri *et al.* [4], reduces the parasitic capacitance of the CPW signal pad. The diameter of this aperture is 320 µm. Another critical feature on the test board is a cutoff mode circular waveguide located under the lower CPW ground plane and centered on the circular aperture. This cutoff waveguide is designed to suppress the radiation from the circular aperture into the lower tape layers of the test board. The circular waveguide has an inner radius of the rings of 230 µm and features a TE11 mode cutoff at approximately 144 GHz. Excited at 60 GHz (77 GHz), the TE11 mode will decay by 20.5 dB (19 dB) over the waveguide's longitudinal length of 324 µm associated with three tape layers. Therefore, this cutoff mode waveguide is effective in suppressing aperture radiation without compromising the decrease in parallel plate capacitance afforded by the aperture. The aperture and cutoff mode circular waveguide are both visible in Fig. 1.

Another key feature of this design is the inclusion of an air pocket located on the edge of the package in the area above the signal via. The pocket is shown in Fig. 3 and measures 1.0 mm wide in the transverse direction and 0.975 mm long in the longitudinal direction. This pocket is fabricated as a cavity in the upper two layers of the four-layer LTCC package. The purpose of this air cavity is to significantly reduce the coupling of RF power into a parasitic TM mode surface wave that would otherwise propagate across the upper two tape layers of the package. Also shown in Fig. 3 is a U-shaped antipad (shown in red) of 440 µm in diameter located in the stripline upper ground. This antipad decreases the localized parasitic capacitance to ground of the signal via, resulting in an improved broadband match in the via-to-stripline transition.

III. Simulated Performance

This board-to-interposer BGA transition was simulated and optimized using CST Microstripes 2012, which uses a time-domain transmission line matrix method. The simulated performance is shown in the s-parameter graphs in Fig. 4(a) and (b). The simulation model was optimized for performance at 60 GHz, resulting in an insertion loss of better than 0.5 dB at 60 GHz and a return loss of better than 20 dB between 50 and 70 GHz. The transition has a simulated insertion loss of less than 1 dB and a simulated return loss of better than 12 dB up to 80 GHz.

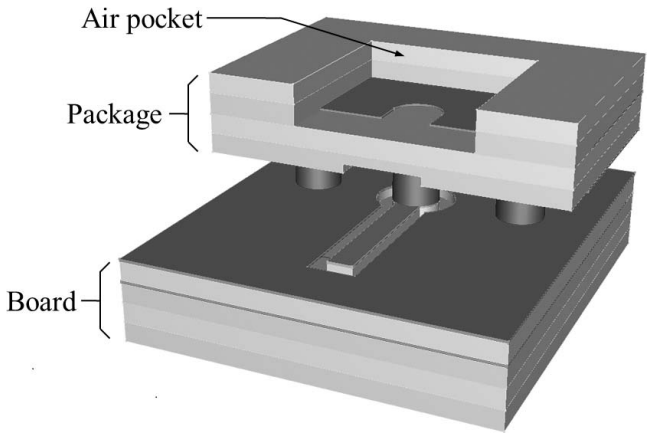

Fig. 3: 3D solid model of the BGA transition design, highlighting the air pocket in the package.

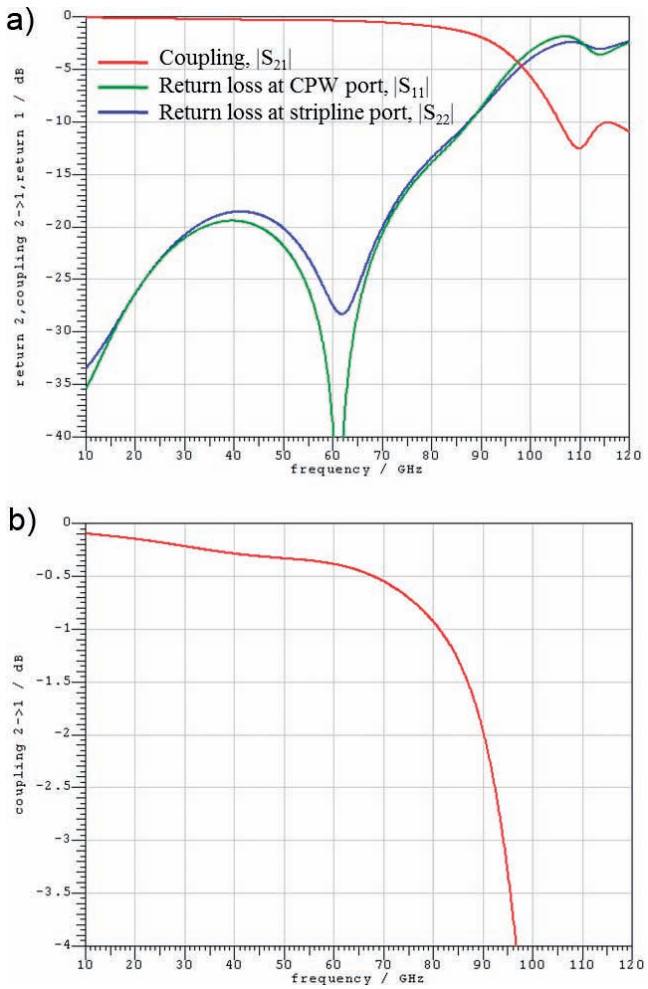

Fig. 4: Simulated s-parameters of the board-to-interposer BGA transition: (a) insertion loss and return loss, (b) detailed view of insertion loss.

Current density throughout the proposed transition was also examined through simulation. Fig. 5(a) features the root mean square (RMS) current distribution plot of the

board-to-interposer transition. Fig. 5(b) showcases the same RMS current distribution but has hidden the upper ground planes of the board and interposer to show the currents flowing on the ground plane below the CPW and on the 50Ω stripline. The simulation reveals currents in the -30 dB range flowing along the edges of the interposer ground plane, representing some parasitic current that is carrying power away from the transmission lines. The two vias oriented along the transverse edge of the interposer on either side of the longitudinal rows of shielding vias were added to decrease the magnitude of this parasitic current flowing along the ground plane edge. Currents associated with the CPW mode are well confined within the shielding vias both on the board's top ground layer away from the transition and on the interior ground layer. The currents on the stripline away from the transition appear to be well confined within the row of shielding vias on either side.

Analysis was also performed to evaluate the amount of power dissipated by all the conductive bodies in the proposed transition design. The findings of this analysis are shown in Fig. 6. The 50Ω stripline is the largest source of material loss in the design, dissipating close to 1.2 % of the total incident power at 60 GHz. The two highest loss mechanisms are the 50Ω stripline and the 50Ω CPW center conductor, which can be anticipated due to the high concentration of current in a well-matched system. Despite the solder balls having a much higher resistivity than the thick-film gold conductors in the LTCC, the solder balls are not a main contributor to loss. The signal solder ball is responsible for dissipating approximately 0.2 % of the total incident power, and the individual ground solder balls (not shown in Fig. 6 due to low values) each dissipate < 0.1 % of the incident power.

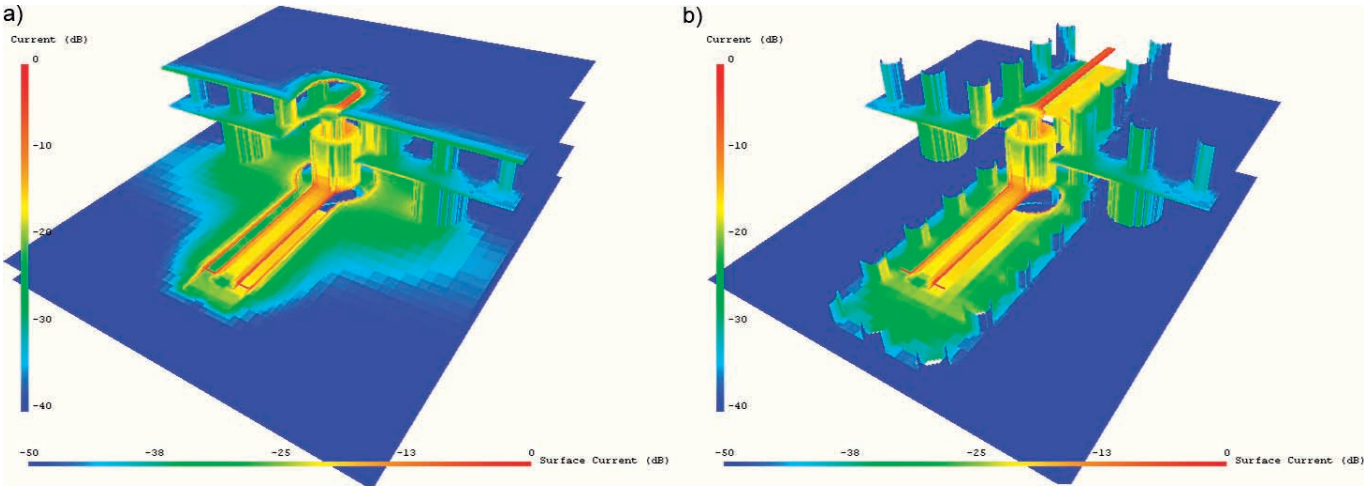

Fig. 5 : Simulated RMS current distribution of (a) the board-to-interposer BGA transition showing all metal surfaces, and (b) the same current distribution plot with the upper ground plane of both the board and interposer hidden.

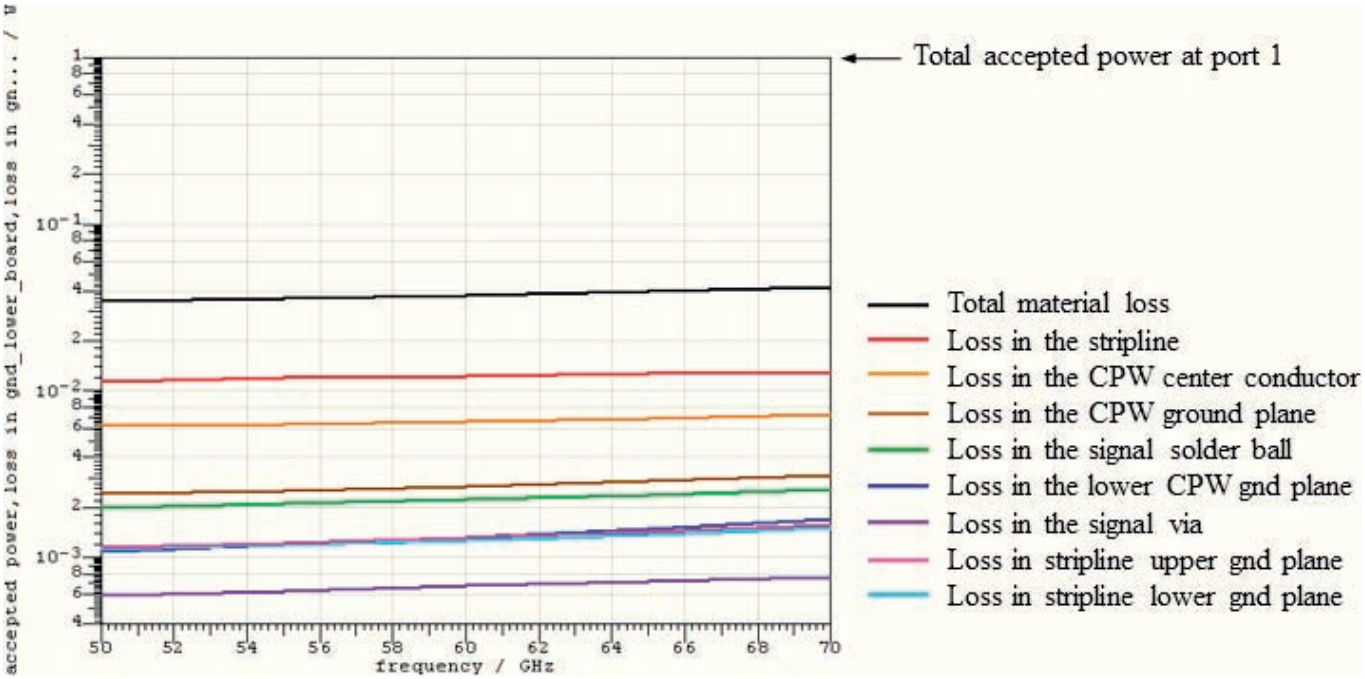

Fig. 6 : Simulation results produced a log plot of the ratio of power dissipated in a given conductive body to the total power accepted at port 1.

IV. Results and Discussion

To test the board-to-interposer interconnect, a back-to-back transition test part was fabricated using 9K7 LTCC for both the board and interposer. The board-to-interposer transition design is mirrored to create the test vehicle, with the two BGA transitions connected by a stripline inside the interposer that measures 2.135 mm in length. A 3D cutaway view of the simulated model for the test vehicle is shown in Fig. 7. The two GCPW launches enable 2-port s-parameter measurements to be taken on the interposer using a network analyzer. Images of both the fabricated individual test structures and the assembled test vehicle are shown in Fig. 8. As seen in Fig. 8(b), the fabricated test vehicle placed a solder ball at each corner of the interposer for mechanical support during attach and reflow. The back-to-back transition test vehicle was modeled and simulated using CST Microstripes 2012.

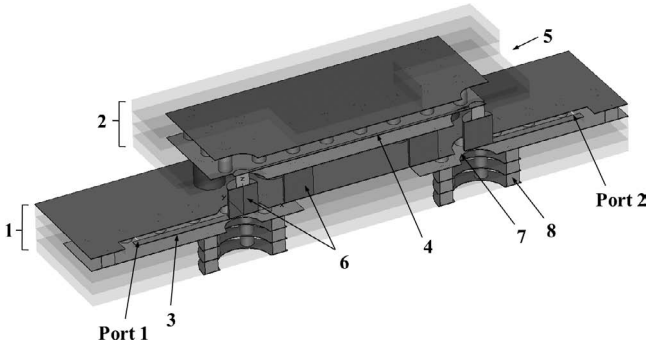

Fig. 7: 3D cutaway view along axis of symmetry of the board-to-interposer BGA transitions test vehicle.

Samples of the assembled back-to-back transition test vehicle were measured using an Anritsu ME828 Vectorstar Vector Network Analyzer (VNA) with millimeter-wave test heads that enable full two port measurements up to 110 GHz. The test structures were wafer probed on a Cascade Microtech S300 probe station using 150-μm GSG probes. Full two-port s-parameter measurements were captured as frequency was swept from 10 MHz up to 90 GHz. Fig. 9 shows measurement results alongside simulation results of (a) insertion loss and (b) return loss of the fully assembled back-to-back BGA transition test vehicle. Full-wave simulation results predict that the assembled package will have less than 1 dB insertion loss at 60 GHz and less than 2 dB insertion loss up to 80 GHz. Measured insertion loss of an assembled package is approximately 2 dB at 60 GHz and less than 4 dB at 80 GHz. Return loss is predicted to be > 9 dB up to 80 GHz and measured results demonstrate > 7.9 dB up to 80 GHz, suggesting a good impedance match throughout the cascaded transitions. In the optimized frequency band between 50 and 80 GHz, measured return loss is better than 10 dB despite increased return loss seen around 60 GHz when compared to simulated results that show better than 13 dB. The test vehicle contained two BGA transitions and a short length of stripline, so the insertion loss per transition can be expected to be a maximum of half of the measured insertion loss. For an individual transition, measured results suggest that it is reasonable to expect less than 2 dB of insertion loss and greater than 10 dB of return loss per transition for frequencies up to 80 GHz. The difference between the ideal cylindrical shape of the solder balls in the simulation and the actual barrel shape of the reflowed solder balls, which will reduce the distance between adjacent solder pillars, is believed to contribute to the difference between simulated and measured results. Alignment of the signal via in the interposer connecting the signal solder pad to the stripline may also contribute some of the variation between simulated and measured results. Cross-sections have suggested that the conductor thickness was moderately thinner than the 10 μm that was defined in the simulations, which could result in higher conductor loss in the signal path than the simulations predict.

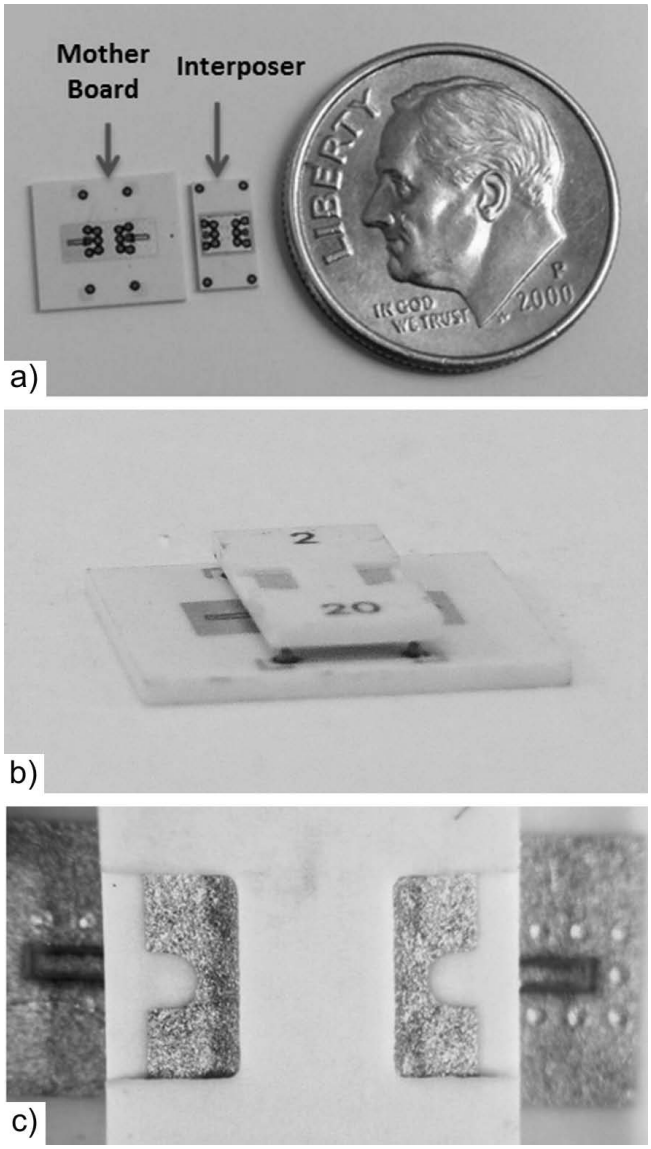

Fig. 8: (a) Individual parts of the board and interposer for the BGA transition test vehicle are shown. (b) An assembled board-to-interposer BGA transition test vehicle is shown from the side and (c) from overhead..

To demonstrate the reliability of the solder ball interconnects, an accelerated aging test was performed on one assembled package by exposing the unit to 85 °C and 85 % relative humidity for 1000 hours. Given the very similar CTE match of 9K7 LTCC and semiconductor materials,

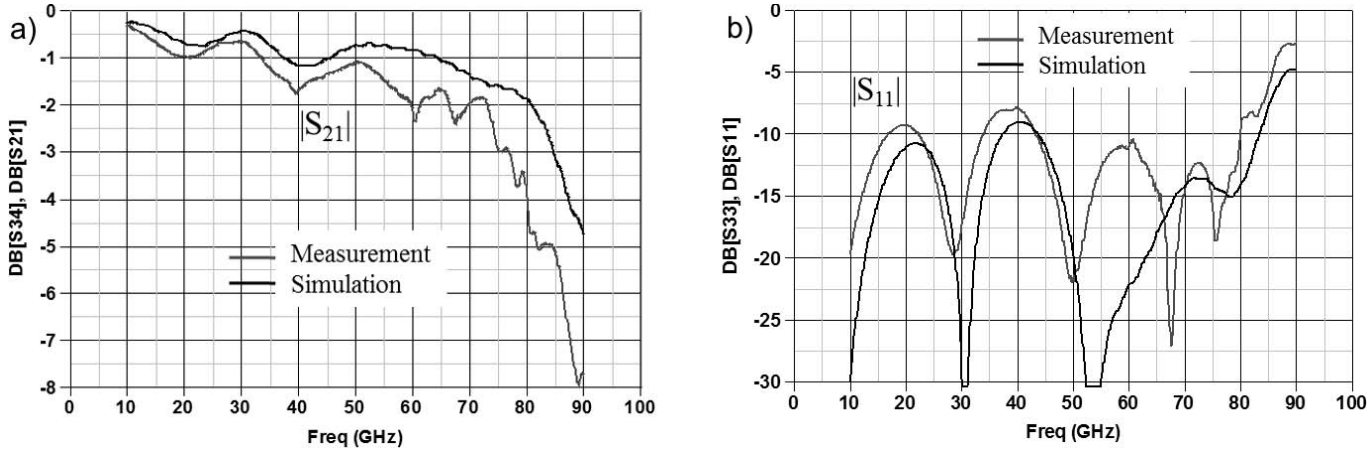

Fig. 9 : Measured and simulated (a) insertion loss and (b) return loss of a back-to-back board-to-interposer BGA transition test vehicle.

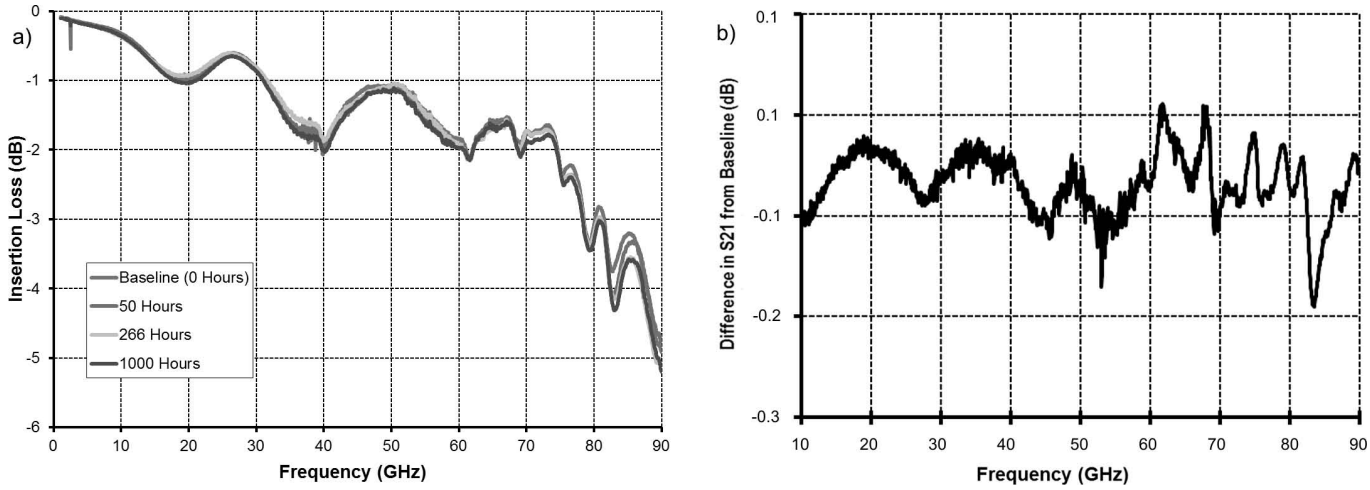

Fig. 10: (a) Insertion loss measurements at various time intervals after 85 °C/85 %RH exposure; (b) difference in insertion loss between the baseline and 1000 hour measurements.

the assembled test vehicle containing the board and interposer provide a realistic comparison to a semiconductor device flip-chipped onto an LTCC interposer. Insertion loss measurements at 0, 50, 266, and 1000 hours of 85/85 exposure are shown in Fig. 10(a). After the 1000-hour exposure, the aged package measured an additional insertion loss of less than 0.1 dB for almost all frequencies up to 90 GHz when compared to its pre-exposure baseline, as shown in Fig. 10(b). The results of this accelerated aging demonstrate the high reliability that can be expected from an LTCC SiP solution.

V. Conclusions

This paper presents a broadband, LTCC board-to-interposer BGA interconnect that demonstrates a measured insertion loss of less than 2 dB per transition up to 80 GHz with greater than 10 dB return loss at most frequencies up to 80 GHz. Interconnect design solutions such as the one presented can provide excellent electrical performance demanded by complex millimeter-wave applications, such as 60 GHz short-range communication systems and 77 GHz automotive radar. Multiple design features have been incorporated into the LTCC board (circular aperture and radiation shield) and into the LTCC interposer (air pocket and the U-shaped antipad in the upper stripline ground plane) to achieve the low insertion loss and wide bandwidth demonstrated by this design.

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