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Materials and Processes of Microelectronic Packaging including Low-Temperature Cofired Ceramics Technology (Past, Present and Future)

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Abstract

As semiconductor technology advances and computers become smaller with higher functionality, the technology has extended into a variety of areas, such as Information Technology (IT)-enabled household electronics, Information Communication Technology (ICT) devices, electronic automobiles and Intelligent Transport Systems (ITS) transport networks, to enrich people's lives. Packaging technology serves as a vital bridge between semiconductor chips and computer systems. Its considerable value is recognized in the constant contributions it makes in bringing about a prosperous life. This paper addresses the two mainstream areas of high-end computers and consumer products, with a special focus on the ceramic materials and process technology of the packaging technologies field at the primary packaging level. Drawing on the past and present developments in these areas as well as future prospects, the paper elucidates the significance of ceramics in packaging including Low-Temperature Cofired Ceramics (LTCC).

Keywords: Low-temperature cofired ceramics (LTCC), microelectronic packaging, flexible electronics, aerosol-type nanoparticle deposition (NPD), embedded passive

I. Introduction

As semiconductor technology advances and computers become smaller with higher functionality, the technology has extended into a variety of areas, such as Information Technology (IT)-enabled household electronics, Information Communication Technology (ICT) devices, electronic automobiles and Intelligent Transport Systems (ITS) transport networks, to enrich people's lives.

With extensive application coverage, packaging technology serves as a vital bridge between semiconductor chips and computer systems. Packages play a vital role of responding adequately to the requests of semiconductor devices and systems.

In general, there are four levels of layers in the packaging for general-purpose computers used in large-scale systems (Fig. 1) [1]. The first level includes the package assembly, which allows the Input/Output (I/O) terminals of semiconductor chips to expand connections via single chip packages or multi-chip modules (MCMs). The second level includes the assembly of various parts and packages onto the Printed Wiring Board (PWB). The third level involves interconnecting PWBs through backplane wiring. The fourth is to mount the whole unit onto a rack, where the backplane connections extend through the rack. The primary level of packaging technology addressed in this paper is the first level.

Fig. 2 depicts a typical assembly structure of levels 1 and 2 packaging. It is composed of the circuit board (wiring, insulator), electronic parts, heat dissipation parts and interconnections. The I/O terminals of silicone-based Large Scale Integrated Circuit (LSI) and the decoupling capacitors made from high-performance dielectric ceramics are soldered onto the external metal terminals of ceramic/plastic packaging (e.g., ceramics: Low Temperature Cofired Ceramics (LTCC)), and mounted onto the resin board. The silicone is connected to a heat sink or heat spreader at the back via Thermal Interface Material (TIM) to lower the contact thermal resistance and enhance the LSI's heat dissipation performance.

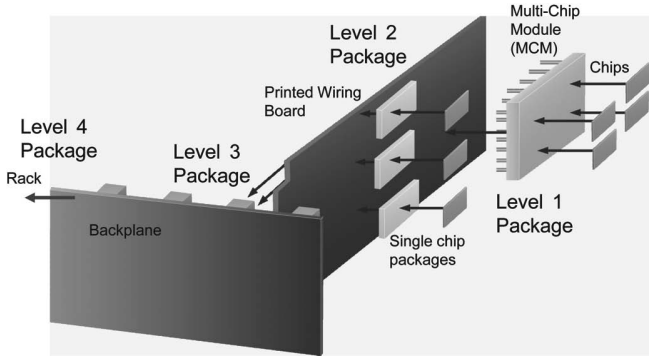

Fig. 1: Package hierarchy.

The package design, structure/format and materials must meet various requirements in order to satisfy the assembly specifications, which depend on the system specifications. There are mainly three materials used in packaging technology: metal, ceramics and resin. These materials differ from one another in terms of electrical (conduc-

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tivity, insulation/inductivity), thermal (thermal conductivity, thermal expansion, heat resistance), and mechanical (moldability, strength) properties, which are relevant to the packaging technology. Therefore, it is necessary to leverage the advantages of each material to integrate them into packaging. If a combination of standard materials is insufficient to meet the specification requirements, the need for a new, breakthrough technology arises, leading to explorations for new materials and processes to arrive at new technologies.

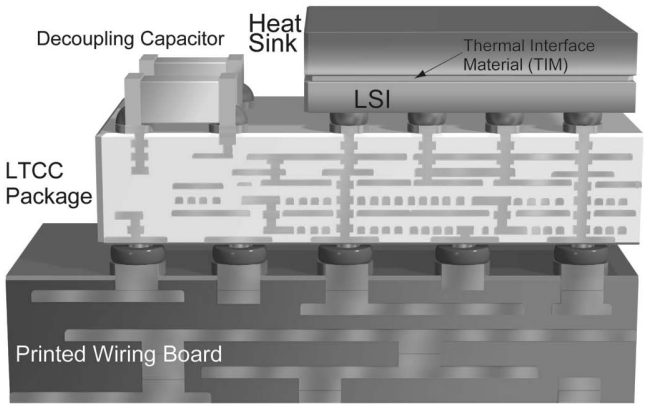

Fig. 2: Typical package structure in high-speed computer.

The recent trends in computing are beginning to divide into two directions. One such direction concerns performance-centered high-end computers, such as supercomputers (often employed in predictions in science technology, medicine, meteorology and global environment to support innovations) and datacenter high-speed servers (used for cloud computing systems aimed at efficiently handling Big Data). The other such direction concerns low-cost consumer products, including smartphones and tablet Personal Computers (PCs). Until today, packaging technology has focused on maximizing the performance of active components. However, it is increasingly important now to directly respond to system requirements and market needs.

This paper describes past and present developments with respect to the ceramics material/process technology that brings the unique, irreplaceable characteristics of ceramics to both the trends in electronics packaging. It also discusses the future prospects of such developments.

II. High-End Computers

(1) PWB integration reaching the limit (move toward ceramic boards)

The value of ceramic materials was first recognized in the domain of packaging technology in the 1980s. Prior thereto, the packaging boards for large general-purpose computers consisted of resin PWBs. Those days, printed boards that were densely mounted with highly-integrated LSIs for faster computing were susceptible to heat due to the resin board being exposed to the heat dissipated from the LSIs, posing a crucial challenge to addressing the thermal instability of the resin. Additionally, the circuit density was limited by the machining technology of drilling on the circuit board. Thus, integration on the resin board, which had a large thermal expansion coefficient, was approaching the limit as the LSI density largely depended on the differences between the thermal expansion of the base material and silicone. Against this background, Fujitsu developed a PWB with highly enhanced plastic material and process technology (see Fig. 3) in 1981, and deployed it in the large general-purpose computers M-380 and M-780.

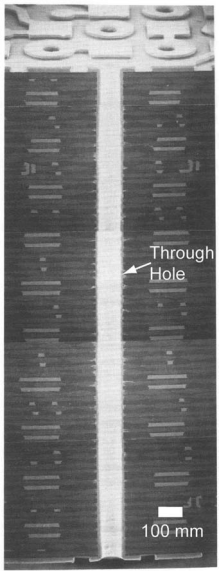

Fig. 3: Cross-sectional view of printed wiring board of mainframe computer FACOM M-780 (540 × 488 mm, thickness: 7.3 mm, layer: 42, through-hole diameter: 120 μm).

Meanwhile, IBM brought to the market a large computer, the IBM 3081 [2], which employed packaging of unprecedented integration density. This multi-layer package, called Thermal Conduction Module (TCM), was a 9 x 9 cm alumina-base board with 33 layers integrating approximately 4500 circuits, which was equipped with a liquid cooling heat-conducting jacket for cooling the components (see Fig. 4). Internally, there were 10000 via holes, 0.125 mm in diameter, and the board had a total wiring length of 120 m [3]. This was the ultimate alumina-based multi-layer circuit board at the time.

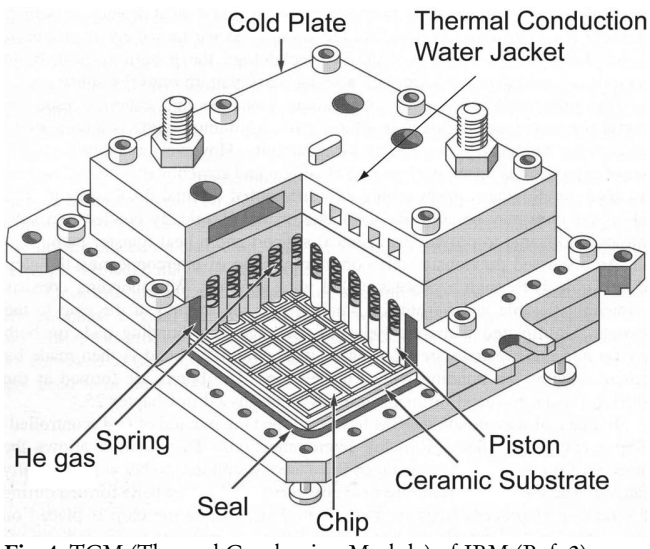

Fig. 4: TCM (Thermal Conduction Module) of IBM (Ref. 2).

Contemporary Japanese engineers who were engaged in packaging technology were impressed by IBM's TCM, but remained skeptical to an extent about the alumina-base ceramic board [4]. The reason was as follows: ceramic boards had a potential for higher package density compared to plastic boards, but current alumina-base ceramic boards had a high permittivity, which meant that the signal propagation time did not improve as much as the enhanced package density. The ceramic board required about twice as much time for signal propagation as that of the printed board. In order to achieve the same level of propagation time, it had to halve the wiring length, which in turn would give rise to the issue of heat generation. There was an awareness that a new ceramic-based circuit board had to be developed, which applied a material with smaller permittivity than the alumina-based material, for the next-generation high-speed computers.

In order to realize a package with LSI's mounting pitch highly densified and wiring length shortened, a minute wiring circuit needs to be formed. The alumina-based ceramic board uses molybdenum (Mo) and tungsten (W) whose electric resistance is high, thus making it difficult to downsize the wiring. In order to integrate the wiring on the board and increase the number of LSIs to be mounted on the same board, multi-layering and scaling up are inevitable. To make this happen, it is necessary to minimize the transmission loss due to the increased total wiring length within the circuit board, for which it is crucial to select a conductor with low electric resistance. Furthermore, there is a need for a circuit board material that is more compatible with (silicone) devices with regard to the coefficient of thermal expansion, in order to package devices into more minutely wired circuits. For faster signal propagation, it is also necessary to lower the permittivity of the insulation layers surrounding the signal wiring. The task at hand was to develop the material and board that met all the above requirements, that is, to develop a large, ultra-multilayer board that combined low-permittivity ceramics that were closer to silicone in thermal expansion characteristics, and a low-resistance conductor.

Fujitsu then successfully announced a large, ultra-multilayer ceramic circuit board, incorporating a thick-film copper conductor for mainframe computers in 1988, before IBM (1990). Fujitsu's circuit board (Fig. 5) was a glass/alumina compound base, 245-mm square with 61 layers (including 36 signal layers, with a total wiring length of 1 km), and a mounting capacity of up to 144 LSIs, using LTCC [5]. Incidentally, the circuit board by IBM was 127.5-mm square, with 63 copper-wired layers and a mounting capacity of 121 LSIs. Fig. 6 depicts the typical manufacturing process of a multilayer ceramic board. A mixture of ingredients (ceramics powder, organic resin and solvent) is kneaded in a ball mill to form a milk-like ceramics slurry. It is then formed into a green sheet by means of tape casting. The green sheet is cut out with a mold and via holes are made. Additionally, a conductor is embedded in the via holes, onto which wiring patterns are printed by means of screen printing. A number of green sheets thus formed of conductors are heated and compressed to obtain the laminated green sheets. Subsequently, the conductors in the laminate and ceramics are fired simultaneously to complete the fabrication of the multilayer board [6]. If copper wiring is introduced, the calcination oxygen level must be carefully controlled through the firing process to promote oxidation to remove the organic resin, which is used in forming the ceramic board, and to prevent the oxidation of the copper. An optimal firing atmosphere was identified for both stable copper reduction and carbon oxidation, as shown in Fig. 7. This manufacturing method is called the green sheet method, and is applied, for example, to ceramic chip capacitors. Today, this technology continues to be employed by Fujitsu and IBM for supercomputer packages.

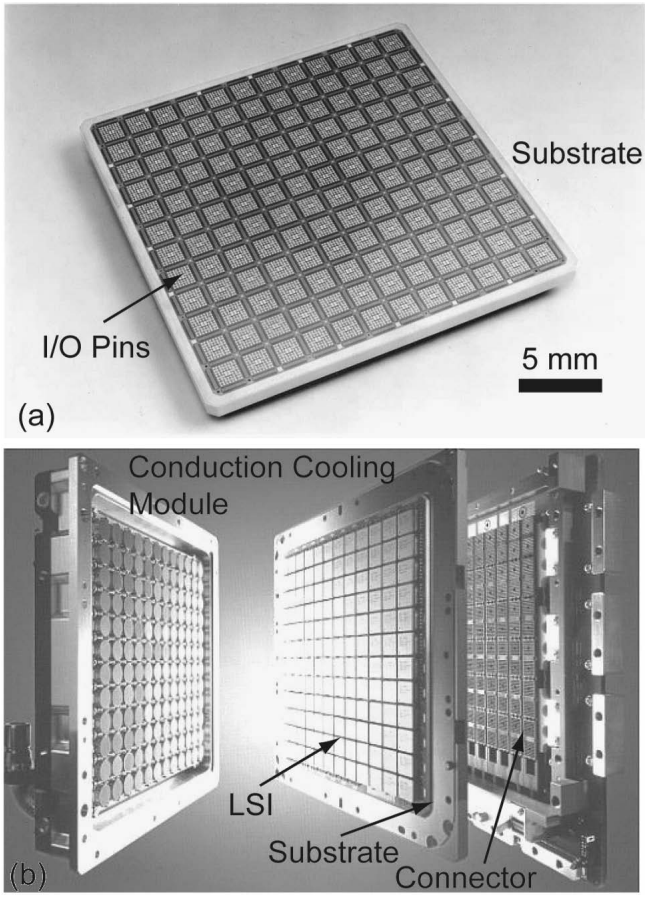

Fig. 5: (a) Multilayer ceramic circuit board for mainframe computer (245 × 245 mm, thickness: 13 mm, layer: 61, pattern width: 80 μm, via diameter: 50 μm), (b) Conduction cooling module.

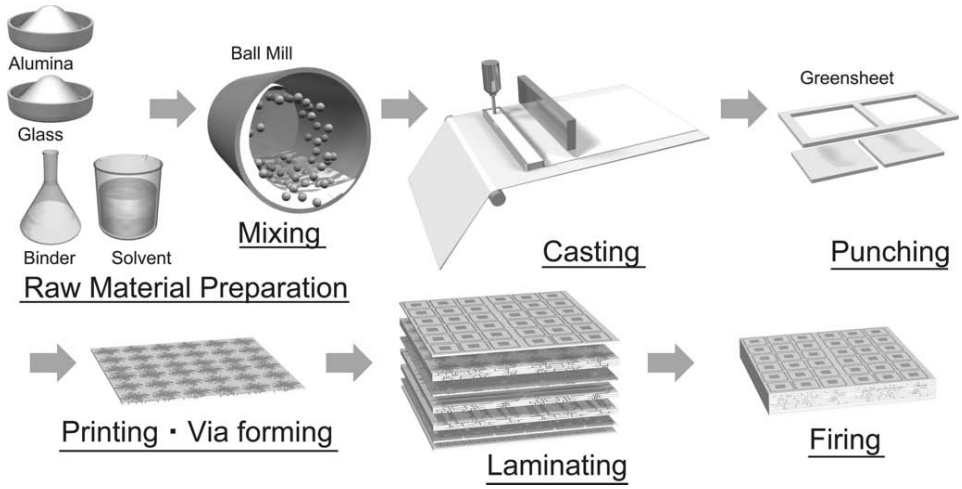

Fig. 6: Typical manufacturing process for ceramic circuit board.

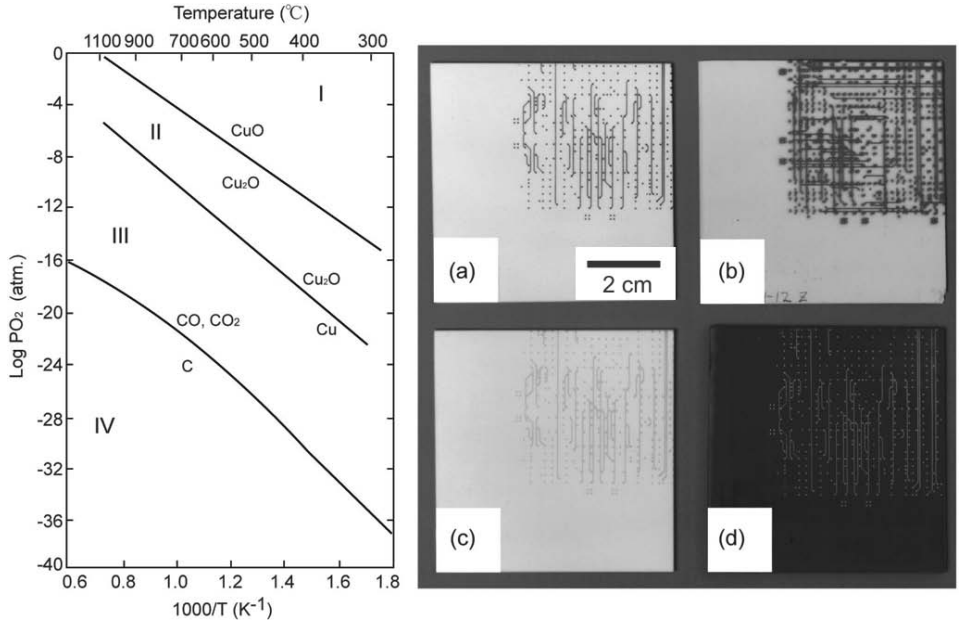

Fig. 7: Cu/Ceramic state in various firing atmospheres (a) CuO/CO, CO_2 (I), (b) Cu_2O/CO, CO_2 (II), (c) Cu/CO, CO_2 (III), (d) Cu/C (IV).

(2) Bipolar transistor calorific value approaching the limit (move toward Complementary Metal Oxide Semiconductor (CMOS))

The bipolar transistor was the mainstream for improving computing speed until the mid-1990s. This transistor controls switching and amplification by input current. As high integration advanced, calorific values of the devices increased, posing difficulties in system development even when introducing ceramic boards equipped with thermal conductor modules. This led to the development of the low-power semiconductor CMOS. As a result of the rapid advancement of downscaling and integration technologies, a new CMOS emerged that had faster computing capability than conventional bipolar transistors. IBM announced a mainframe computer with a CMOS processor in 1994. This technological innovation regarding semiconductor chips brought a significant change with regard to the form of circuit board packaging for high-end computers. Previously, a single-board Central Processing Unit (CPU) with many bipolar devices was in great demand. The trend shifted toward short, minute wiring between devices to transmit signals without attenuation after integrated CMOS gained popularity due to advanced scaling technology. Gradually, the CMOS device MCM became the primary form of circuit board for high-end computers [7]. This board had sputtered copper wiring. For the insulation, polyimide was used for its compatibility with thin-film copper wiring and multi-layer capability (Fig. 8).

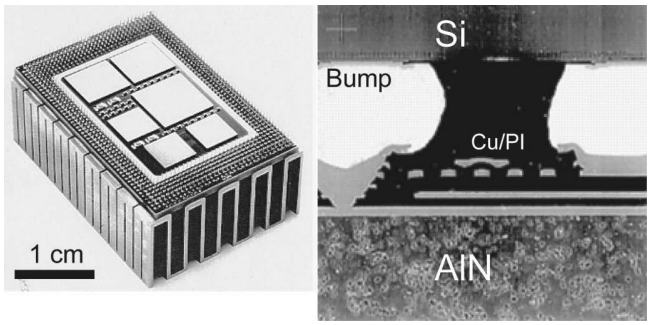

Fig. 8: Multi-chip module (wiring : 5 μm, via diameter: 20 μm).

Ceramics were incorporated as a supporting substrate and heat spreader. In this regard, ceramics were chosen for their high thermal conductivity and low thermal expansion properties, as well as smooth surface and high strength [8]. In 1995, Fujitsu launched GS 8600 followed by GS 800. Both had circuit boards in aluminum nitride (with via), while the main material for the circuit boards was not ceramics, but resin polyimide. Subsequently, demands to cut costs drove some high-speed servers to make a shift from the polyimide thin-film multi-layer boards to resin build-up boards which applied further advanced scaling technology.

(3) CMOS calorific value approaching the limit

CMOS requires electric power when the theoretical value changes (0 to 1) in order to charge or discharge the internal capacitor, but in principle, it does not use electric power while the theoretical value is maintained, thus keeping the power consumption low. The power consumption of transistors is proportionate to a multiplier of capacitance, square of drive voltage and operating frequency. As gate lengths become shortened in order to realize high frequency operation, transistor drive voltage is reduced according to the scaling rules. However, advanced integration technology meant high transistor density, and thus the power density per chip area was increasing. Today, particularly since 2010, the calorific value of CMOS has risen to 200 W per one chip, giving rise to the need to further develop heat dissipation/cooling technology at the packaging level or devices with lower power consumption (Fig. 9) [9].

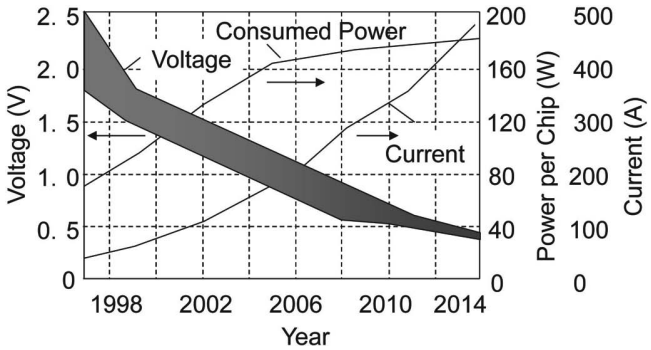

Fig. 9: Change of operating voltage, current and consumed power of high-speed processor in ITRS road map.

This being said, the issues today are not confined to the issue of calorific value. Packages for high-end computers also need to improve with regard to the following three areas: Signal Integrity (SI), Electro Magnetic Interference (EMI) and Power Integrity (PI). SI addresses the preservation of signal waves to maintain the quality of signal propagation, and is highly relevant to the technology for designing and manufacturing transmission wires and peripherals. EMI refers to the interference caused by a pseudo-antenna engendered in areas of high current concentration, such as interconnections inside packages. It is generally dealt with by means of a metal/magnetic shield to prevent the electromagnetic wave from passing. PI is about providing stable power while reducing noise generated in the power system. The need to improve this aspect in tandem with the trend in lowering drive voltage has been increasingly recognized in recent years. In order to reduce the noise in the power system, it is necessary to keep the power line impedance below the target impedance level (Z_{target} = (power voltage, ripple tolerance)/current). Requirements for target impedance are in decline as shown in Fig. 10. An effective way to minimize the power impedance is to place the decoupling capacitor parallel to the power supply line in the immediate vicinity of LSI. To satisfy this requirement, Fujitsu developed the manufacturing process of low-impedance multilayer capacitors with a through via structure that can be directly connected to I/O terminals of LSI.

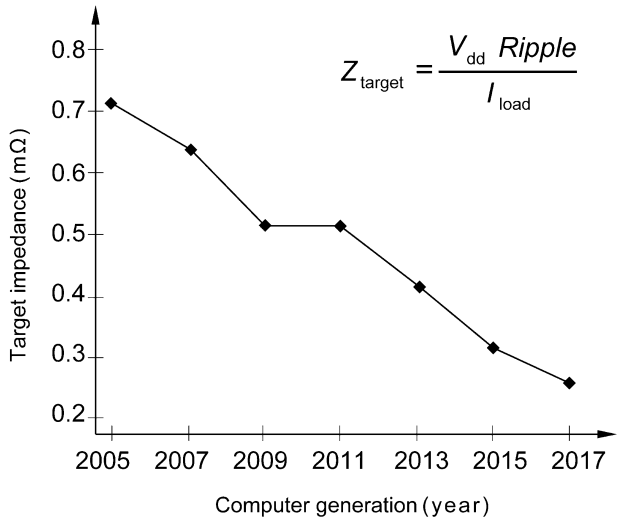

Fig. 10: Target power supply impedance of high-speed processor.

Fig. 11 depicts the process flow. Firstly, form a film of barium titanium oxide on a copper leaf using aerosol-type Nanoparticle Deposition (NPD) (a).

Make via holes using chemical or dry etching (b). Make vias and internal electrodes by copper plating and/or sputtering (c), (d). Repeat the stages to form a multi-layer structure (e). NPD is the core technology for this process. It is an improved version of the aerosol deposition method. The deposition equipment is outlined in Fig. 12. A mechanical vibration process is applied to the ceramic material in preparation, and gas is injected into the material reservoir to blow up micro particles into the gas to create aerosol (mixture of the gas and particles). This aerosol will then be deposited onto the board through a nozzle to form a film. The deposition chamber is maintained in depressurized conditions with a vacuum pump, which generates an acceleration effect on the particles jetted from the nozzle. In the Aerosol Deposition (AD) method, the material particles crush on impact with the board surface. The method leverages the impact consolidation; new surfaces created through the impact retain high surface energy, and diffusion engendered thereof facilitates strong joining of the particles at low temperature. The particles are joined together in this way to form a film. This leaves considerable stress from the impact inside the film. The NPD method utilizes crush-processed dry ceramic particles, conveyed in gas flow, to be deposited onto circuit boards. This method applies a process to cause the crush of the particles inside the nozzle and multiplies the

particles' surface energy before the impact on the board. Although crystalline disturbance occurs on the particle surface through the crush process, internal stress and deformation are released before the deposition. Therefore, particle crystallization inside the film is satisfactory, enabling the formation of a high-density ceramic film with stable crystallization as well as low internal distortion and stress achieved at room temperature. Together with plating, exposure/development wet processing and other processes, this makes it possible to execute the above-stated process for easy formation of minute vias and electrodes with high precision [10].

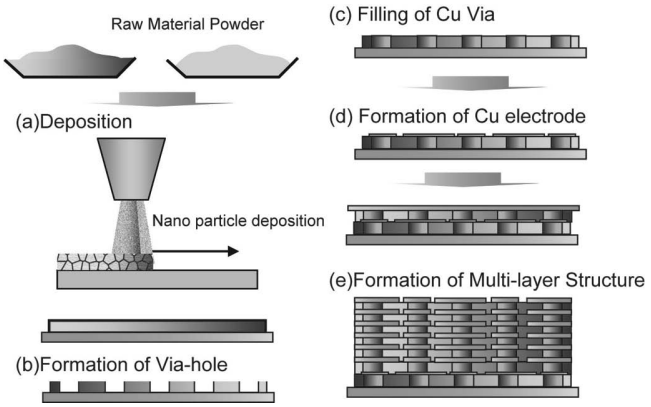

Fig. 11: Manufacturing process of multilayer capacitor with low impedance.

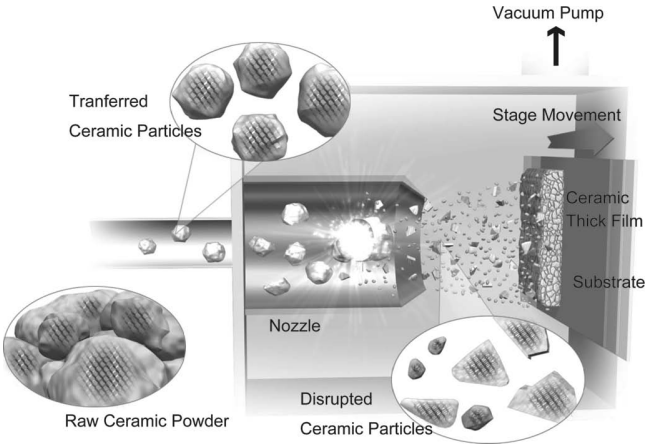

Fig. 12: Schematics of aerosol-type nanoparticle deposition equipment.

III. Consumer Products

The packaging technology for consumer products takes an approach that focuses on size and thickness reduction, as seen in high-density surface mount technology (SMT). It is preferred if the end-products are commoditized at low cost. Various bonding methods have been developed to realize high density integration of electronic devices at low cost, such as wire bonding, tape automated bonding (TAB), and (in tandem with the design change regarding the I/O terminals of IC) flip chip bonding. It was the hybrid IC technology that brought ceramics into the packaging technology for consumer products. This technology facilitates package downscaling by screen printing patterns on alumina-base ceramic boards using ink paste to form layers consisting of the conductor, dielectric, resistive element and overcoat glass film, which then undergo calcification at 900 °C to create IC substrate, onto which electronic devices are mounted. The technology continues to advance, and today it develops into resin build-up boards with the application of high-density SMT.

(1) Component-embedded boards

As cellphones have moved toward being multi-functional since the mid-2000s, the technology thereof was innovated to include features such as TV viewing, Global Positioning System (GPS), high-definition cameras, music downloading and various wireless Local Area Network (LAN) devices. These feature modules were mounted onto the plastic build-up boards inside the handsets. In tandem with the pursuit of the multiplication of functions, the industry sought to slim the devices, thereby giving rise to the need for innovation of hardware technology. Module boards were reaching a limit in terms of the capacity to downsize the assembly parts as well as their surface mount density. Thus, new technology was explored to realize downsizing, slimming, higher integration and lower cost (to embed electronic devices in substrates) [11, 12].

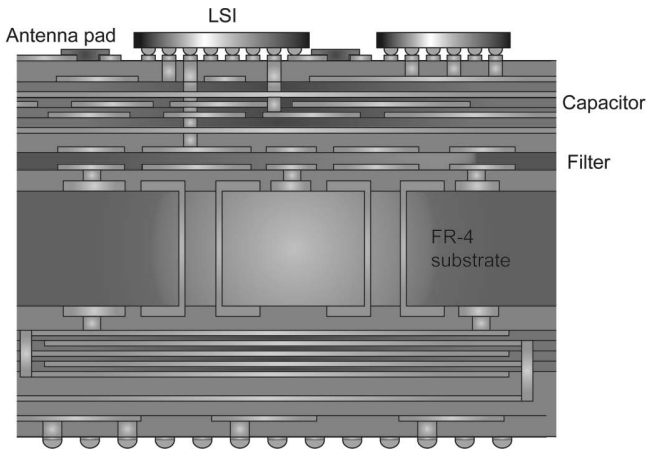

Fig. 13: Target of embedded passive substrate in next generation (cross-section structure).

There are high expectations that the next-generation module boards will be resin boards with embedded ceramic passive devices, such as capacitors, as shown in Fig. 13. However, epoxy substrate can resist heat only up to 200 °C, and it is virtually impossible to embed ceramic films inside the boards, as ceramics must be fired at 1000 °C. Alternatively, resin and ceramic compound would produce material whose permittivity is below 40 and capacitance is at several nF/cm^2, which hardly meets the module specifications.

Leveraging AD, Fujitsu has developed a technology that facilitates ceramic functional film formation inside resin

build-up boards. In order to evaluate the applicability of the capacitor-embedding in resin substrates, a prototype was created to form a multi-layer capacitor on a Flame Retardant Type 4 (FR-4) resin board, as described below. Firstly, the ground layer was prepared by spray painting resist onto a copper leaf on FR-4, which was exposed, developed and etched using photolithography. Secondly, $BaTi0_3$ is deposited using AD over the entire surface of the board, followed by resist application, exposure and development to form a mask pattern. Etching is applied to the AD layer using nitric-hydrofluoric acid. It is followed by the formation of a power layer using Cr/Cu sputter and Cu plating. Furthermore, the process is repeated several times before the final solder resist is formed. Figs. 14 (a) and (b) depict the exterior close up of the multilayered ceramic capacitor formed on FR-4 and its cross-section, respectively. As a result of this prototype, we confirmed that the $BaTiO_3$ AD film formed on FR-4 had comparative permittivity up to 400 and capacitance of 300 nF/cm^2 (maximum) through multi-layering [13–15].

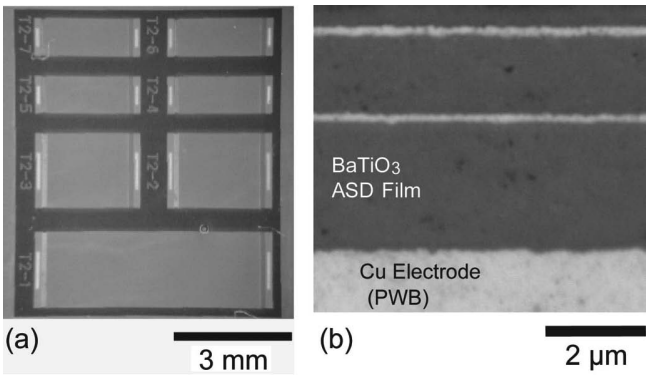

Fig. 14: Multi-layer capacitor formed on FR-4 (a) surface, (b) cross-sectional structure.

(2) Flexible electronics

The recent trend in electronics toward wearable computers is driving electronics towards smaller, thinner devices for next-generation devices that can be thin, lightweight and flexible, so they can be worn in the same manner clothes are. Technology development has been invigorated in recent years in the areas of flexible and stretchable electronics as the core technology [16–19].

With respect to wearable computers, a flexible resin sheet that integrates the circuit network serves as an assembly board. Therefore, functional film for passive devices, such as capacitors and resistors, must be mounted on resin/metal sheets at low temperatures. NPD is an excellent method in terms of electrical properties with the ability to easily form high-quality non-organic films (ceramics/metal) for passive devices onto polyimide films or metal leaves at low temperature, which makes it a viable method for flexible electronics.

The right-hand side of Fig. 15 (a) depicts the film on an aluminum board fabricated by depositing aluminum oxide and barium titanium oxide particles simultaneously. The left-hand side of Fig. 15(a) depicts the internal structure of the film thus fabricated. The microscopic structure of the obtained film is shown in Fig. 15(b). Barium titanium oxide fills the gaps between aluminum particles to form a dense layer of barium titanium oxide particles, joined three-dimensionally within the film (capillaries).

The structure is similar to the internal structure of a barrier layer (BL) capacitor [20] (three-dimensional structure of a thin, high-insulation barrier layer formed on the boundary surface of the sintered material composed of the semiconductor ceramic particles). The main part of the film comprises aggregate metallic aluminum particles, with a layer of barium titanium oxide particles with high permittivity forming the particle boundaries. As shown in Fig. 15 (c), it has been verified that a film of apparent permittivity of 40 000 can be attained by means of deposition at room temperature. The tan δ value is relatively high at this point, but it can be lowered by facilitating further densification of the capillary [21].

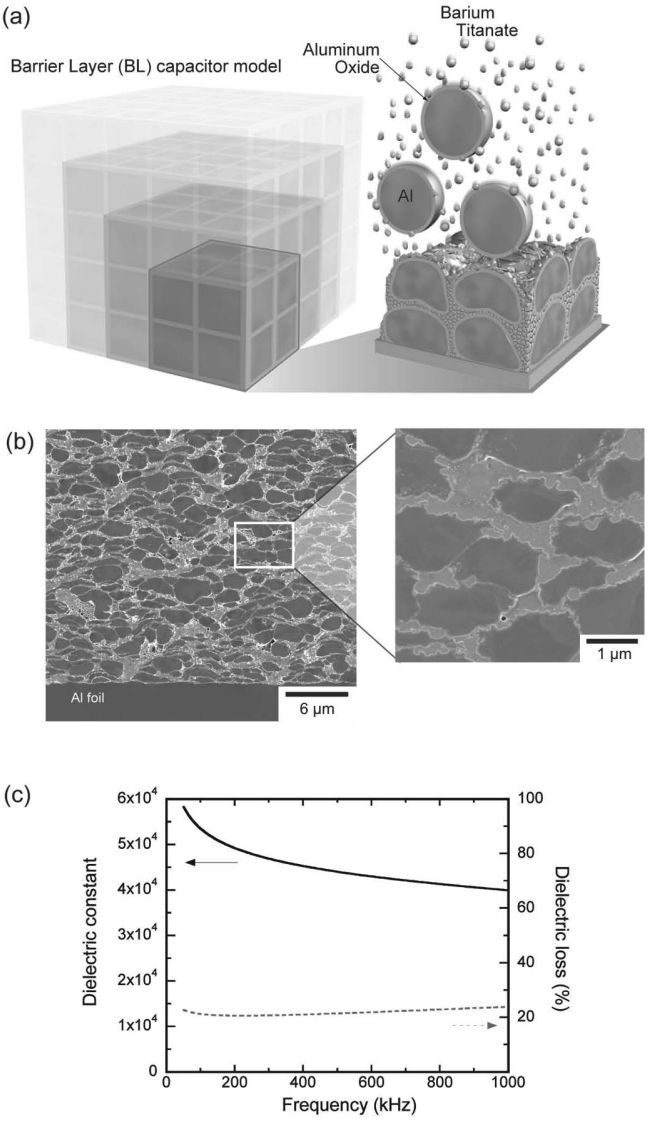

Fig. 15: Structure model: (a) left, manufacturing process: (a) right, microstructure: (b) and dielectric property: (c) of the film with capillary structure.

Because the as-deposited $BaTiO_3$ NPD film is dense, strain- and organic-binder-free, wet photolithography processes such as electric plating and acid-alkali process can be applied to the film before annealing despite the green state.

Fig. 16(a) shows our developed typical manufacturing flow for a multilayered structure with material integration on a Cu foil. First, a ceramic film is deposited on the Cu foil using NPD [22, 23]. The via hole on the as-deposited film can be shaped by chemical etching on the patterned resist using HF/HNO_3, dry etching using reactive ion etching (RIE), etc. The via conductor can be filled using Cu plating, Cu sputtering, and so on. The Cu internal electrode is formed by wet etching a Cu sputter film designed using patterned resist, after the Cu blanket sputter deposition on the as-deposited film has formed the via hole. These processes deposit different ceramic films and form via and internal electrodes, and are repeated to attain the multilayered structure. Finally, the multilayered ceramic structure can be completed by co-annealing the multilayered structure consisting of Cu and various ceramics at around 900 – 1000 °C in nitrogen atmosphere.

Fig. 16(b) shows the 20 μm via hole in the as-deposited film using wet etching by HF/HNO_3. The Cu via conductor can be grown by electric plating from the Cu foil. Fig. 16(c) shows the morphology of the Cu via conductor in a $BaTiO_3$ NPD film annealed at 950 °C. A well-designed via conductor can be constructed even after annealing.

A multilayered structure with various material combinations on a Cu foil can be obtained using this technology. Figs. 16(d) and 16(e) show an as-deposited and a 950 °C-annealed $BaTiO_3/Al_2O_3/Cu$ multilayered structure, respectively. Figs. 16(f) and 16(c) show magnified images of the $BaTiO_3$ and Al_2O_3 parts annealed at 950 °C in nitrogen atmosphere, respectively. This structure is fabricated with the multilayered ceramic process that we developed. The stress-free nanoparticulated alumina film is also densified at 950 °C, below the melting point of Cu (1083 °C), despite the optimum sintering temperature of 1600 °C in bulk alumina ceramics. It is hoped that small circuit module substrates serving various functions, such as capacitor, filter, and so on, will be produced by using the above material combination: low-resistivity conductor (e.g., Cu), low-permittivity dielectrics surrounding the signal line (e.g., alumina), and high-permittivity dielectrics for capacitors (e.g., $BaTiO_3$). Because the multilayered structure is fabricated on Cu foil by using this ceramic process, the structure can be embedded in a resin-based build-up package.

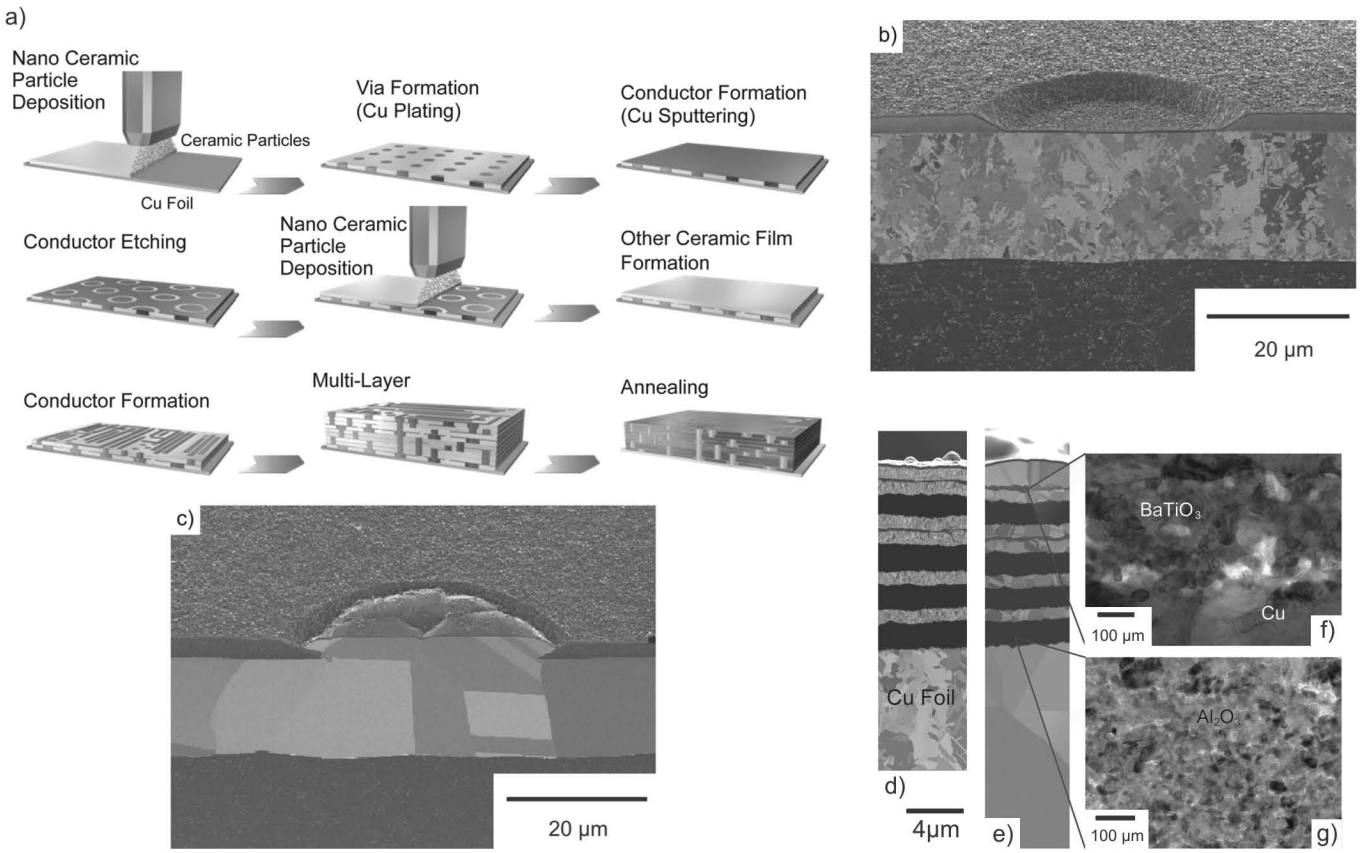

Fig. 16: (a) New ceramic process using aerosol-type nanoparticle deposition for obtaining multilayer structure forming fine copper electrode and vias. (b) Via-hole in as-deposited $BaTiO_3$ NPD film using wet chemical etching, (c) Cu conductor via filled with electric plating after co-annealing at 950 °C. (d) $BaTiO_3/Al_2O_3/Cu$ multi-layered structure consisting of as-deposited film and sputtered Cu on Cu foil using NPD. (e) $BaTiO_3/Al_2O_3/Cu$ multi-layered structure annealed at 950 °C in nitrogen atmosphere. Magnified densified ceramic layers after annealing: (f) $BaTiO_3$ layer, (g) Al_2O_3 layer.

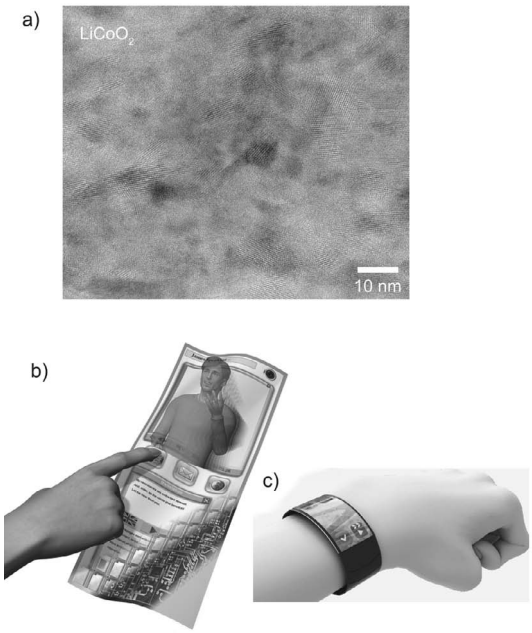

Fig. 17: (a) Internal structure of $LiCoO_2$ film for lithium ion battery (b) Image of wearable communication device applying flexible electronics (c) Smart watch using flexible electronics.

This method of deposition realizes the deposition of highly crystallizing, nano-particulate film onto a surface that is free of resin binder. Therefore, the technology may also be applied to the electrodes of fast-charging lithium-ion batteries. In order to facilitate fast charging, the chemical reaction speed must be enhanced between the electrode material and electrolyte. It is effective to decrease the size of particles for the electrode materials in order to improve the reactivity. Tape casting is widely deployed in fabricating the film for making electrodes, where insular resin binder is added in the process of molding. In general, the smaller the particle's diameter, the more binder is required for molding. This would then lower the proportion of the electrode material in volume and result in a lower contact volume with electrolytes. For this reason, making material particles smaller did not yield much effect in fast charging for conventional methods. As seen in Fig. 17, the $LiCoO_2$ film for positive electrodes of lithium-ion battery fabricated using this technology has a structure composed of particles only a few nanometers in diameter, and it does not contain a resin binder. The crystal structure of the $LiCoO_2$ is maintained in good condition without grid defects. We verified that fast charging was successfully executed with a lithium-ion battery that had the film used on its positive electrode. Furthermore, flexible batteries can be fabricated by making a layer of solid electrolytes laid out in succession on the positive electrode layer on a metallic sheet.

In summation, NPD technology has great potential for making passive devices and thin-film batteries for flexible/stretchable electronics, owing to its ability to integrate ceramics/metal crystalline film on resin/metallic sheets while controlling the inner structure. It can also be applied to oxide electronics, such as ZnO [24], and is viable for embedding positive devices. This makes the technology a key technology for realizing a small, light and thin flexible wearable computer (Fig. 17(b): illustrating a paper-thin device that can be bent easily; comes with many features, such as 3D display, automatic translation suite and other applications; and is useful for communicating with people overseas, Fig. 17(c): smart watch using flexible electronics).

IV. Conclusions

Packaging technology serves as a bridge between electronic devices and computer systems, by accepting external requests to pass onto them, and also conveying the requests from the devices to the systems. Where there is consecutiveness in external needs and technologies, it is not difficult to have a future projection of packaging technology, as certain technology can form a core and dictate a roadmap to respond to technical requirements. However, market needs are in constant flux, as has been described in this paper. It continues to be important to respond to the external needs and develop innovative packaging technology in a timely fashion.

In the future, we anticipate developments will be made not only in the field addressed in this paper, but also in the power electronics of the environment and energy area, and in the high-frequency technologies that are closely related to aerospace and transport systems. We consider that ceramics-based packaging technology is indispensable to each of these areas. We are confident that the ceramic materials and process technologies will continue to play a key role in microelectronics package assembly [25].

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